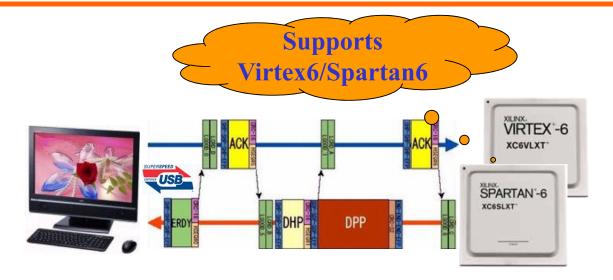




USB3.0 Host & Device IP





Enchant your product with SuperSpeed!

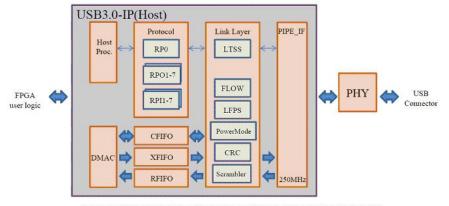
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USB3.0-IP Core intruduction

- IP Core to support USB3.0 SuperSpeed for Host (USB3H-IP) or Device (USB3D-IP)
- Includes Protocol&Link Layer as well as DMAC,Host I/F, and PIPE I/F
- Practical implementation is provided by reference design.







USB3.0-IP Core merit1

- Supports SuperSpeed(5.0Gbps) of USB3.0 Standard.
- Provides controller function of either Host or Device side.
- Connects with external PHY device. (TUSB1310A of T.I)
- Includes USB3.0 PIPE interface. (250MHz@16bit)
- Saves FPGA resource usage by limiting SuperSpeed only.

Device-IP Core (USB3D-IP)	Family	Example Device	Fmax (MHz)	Sireel	IOB:	GCLK	BRAM	MULT7 DSP48/E	DCM / CMT	Design Tools
(00000-197	Spartan*6 (LXT)	XC6SLX45T-3FGG484	182	2582	68	2	9	0	2	ISE® 12.3i
Host-IP Core (USB3H-IP)	Family	Example Device	Fmax (MHz)	Slices1	IOB:	GCLK	BRAM	MULT7 DSP48/E	DCM / CMT	Design Tools
	Spartan*6 (LXT)	XC6SLX45T-3FGG484	180	2627	70	2	9	0	2	ISE • 12.3i

USB3.0-IP resourc report (1 Control, 2 IN/OUT each)

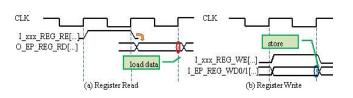
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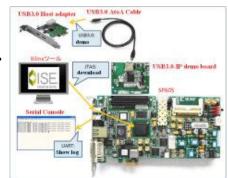




USB3.0-IP Core merit2

- Supports 15 IN/OUT Endpoints at maximum.
 - 1 Control Endpoint
 - 7 IN/OUT Endpoints each at maximum.
- Supports all transport type.
 - (Control/Bulk/Isochronous/Interrupt)
- · Real board evaluation with Xilinx FPGA board
 - (Both Host-IP and Device-IP)
- Simple and easy connection user I/F.





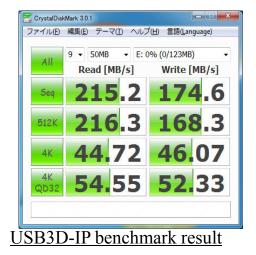
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Device-IP Core performance

- Best performance in existing USB3.0 system.
 - High performance at both sequential and random access.
 - Provides design that minimizes overhead.





(Reference: competitor result)

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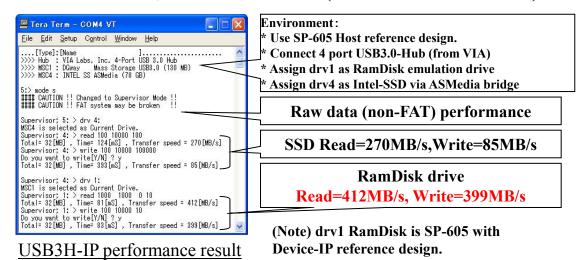
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Host-IP Core performance

- Extracts SuperSpeed upper limit!
 - Raw sequential access (non-FAT) result:
 - Read=412MB/s, Write=399MB/s (use USB3.0 RamDisk)







Core product line up

· Supported FPGA and Core product

Product Info.	Spartan-6	Virtex-6			
Device-IP Core	USB3D-IP002	USB3D-IP003			
Host-IP Core	USB3H-IP002	USB3H-IP003			



- Next product plan
 - Support Virtex-7/Kintex-7/Artix-7



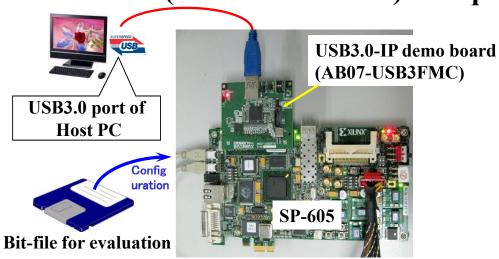
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Evaluation bit-file for Spartan-6

- Free bit-file for evaluation using SP-605
- Demo board (AB07-USB3FMC) is required



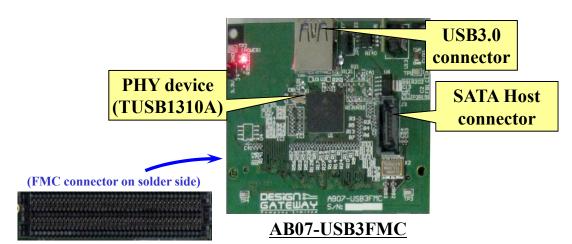
USB3.0-IP evaluation environment





Demo board (AB07-USB3FMC)

- Connects with FMC on SP-605/ML-605
- Mounts TUSB1310A (T.I) and peripheral circuit
- Mounts additional SATA Host connector



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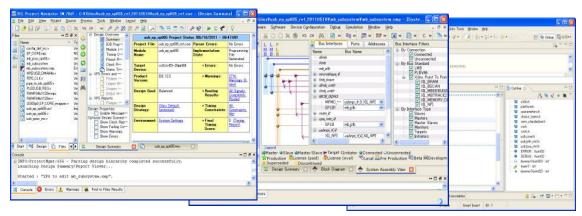
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Reference Design (Summary)

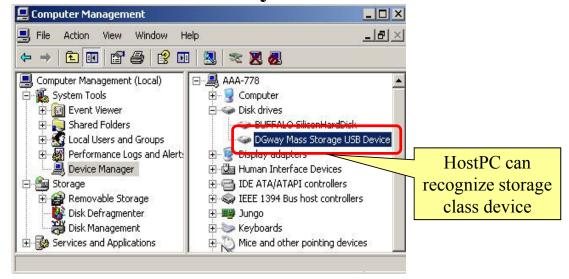
- Real operation on SP-605/ML-605 and demo board.
 - ISE/EDK/SDK project of evaluation bit-file
- Provides all HDL source code except IP-Core.
 - Also provides MicroBlaze firmware by C source





Reference Design (Device function)

- HostPC can recognize storage class device
- Emulate RamDisk by DDR3 on SP-605



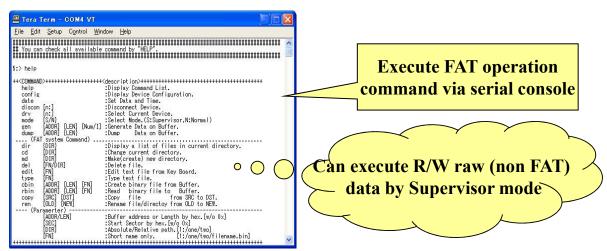
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Reference Design (Host function)

- Access to USB3.0 storage device by FAT16
- Issue command from serial console



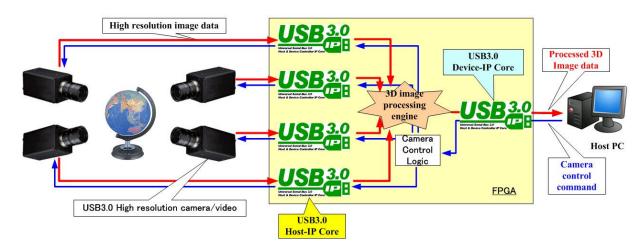
<u>FAT operation menu of Host reference design</u>





Application example1

- Connect multiple high-resolution USB3.0 camera/video
- 3D process in FPGA and send data to PC via USB3.0



High resolution 3D image processing system

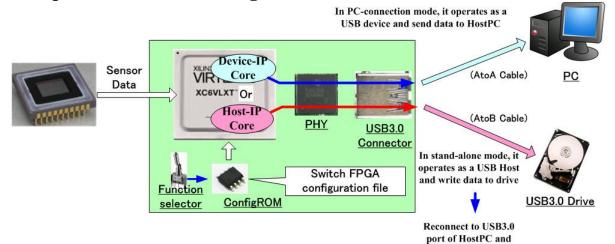
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Application Example 2

- 'Dual Role' system that can operate both PC-connection and stand-alone environment
- Prepare individual configuration data for Host/Device function



Dual Role measurement system

transfer data





Inquiry

- Detailed technical information on Web site
- http://www.design-gateway.com/ or
- http://www.dgway.com/products/IP/USB3-IP/index-E.html
- Inquiry
 - Design Gateway Co.,Ltd.
 - E-mail: sales@design-gateway.com
 - FAX: +662-261-2290





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Revision History

Rev.	Date	Description
1.7XE	2012/07/11	Release English presentation