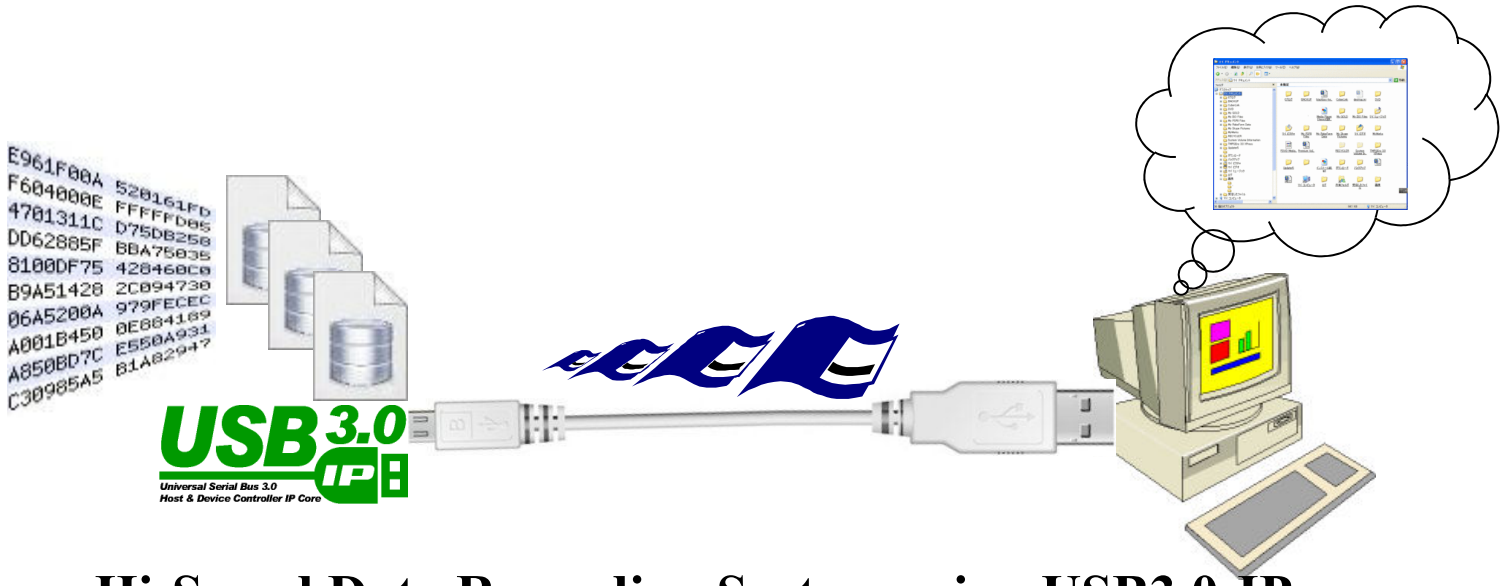
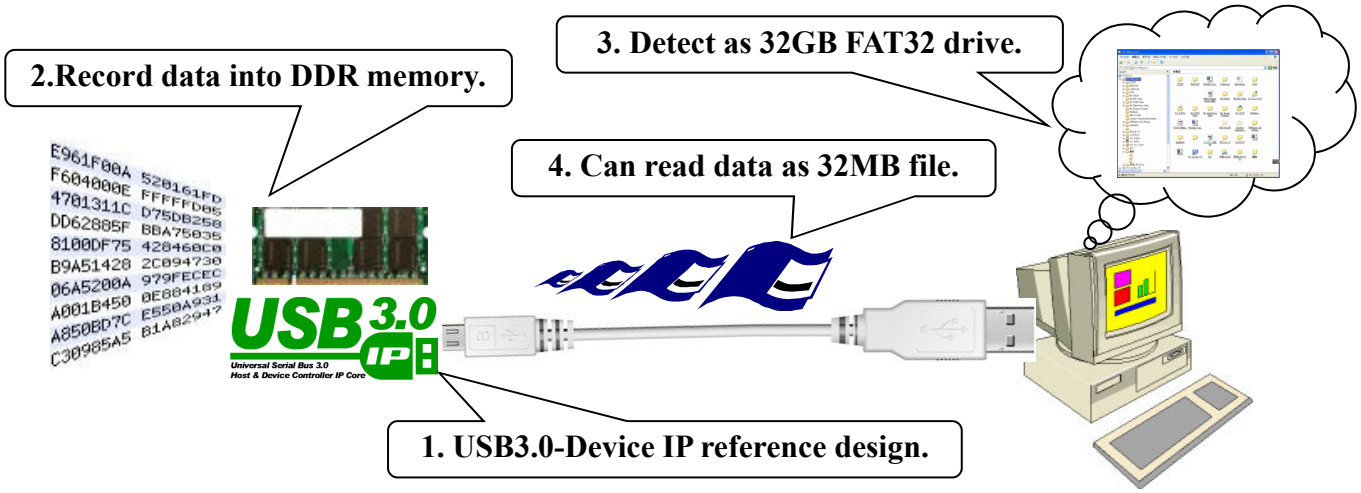
USB3.0-IP FAT32 Data Recorder introduction Ver1.0E



Hi-Speed Data Recording System using USB3.0-IP

What is USB3.0-IP FAT32 Data Recorder?

1. USB3.0 Device IP-Core Reference Design.
2. Record data into DDR memory at FPGA side.
3. Connected PC detects as 32GB general FAT32 drive.
4. User can access to recorded data as 32MB data file.

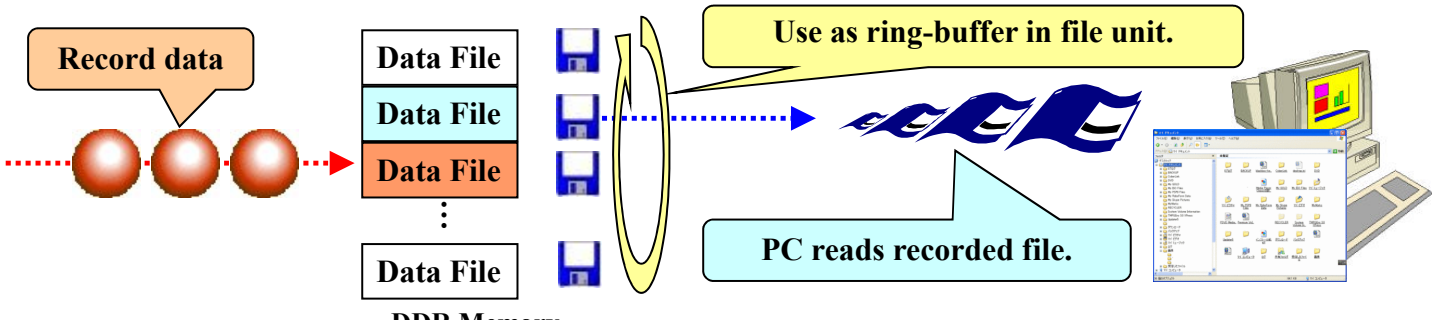


Summary

- User can access recorded data via file system.
  - PC can detect general FAT32 drive, so no special driver required.
  - User can use standard fopen() or fread() funcion, easy to build application.
- High Speed access via USB3.0 interface.
  - USB3.0 in general PC enables high speed data recorder system.
- Full design project including source code with real board operation.
  - Design project for FPGA evaluation board with USB adapter board.
  - User can confirm real operation using design project.
  - Complete source code except IP-Core.
  - Supports latest Altera/Xilinx device family.

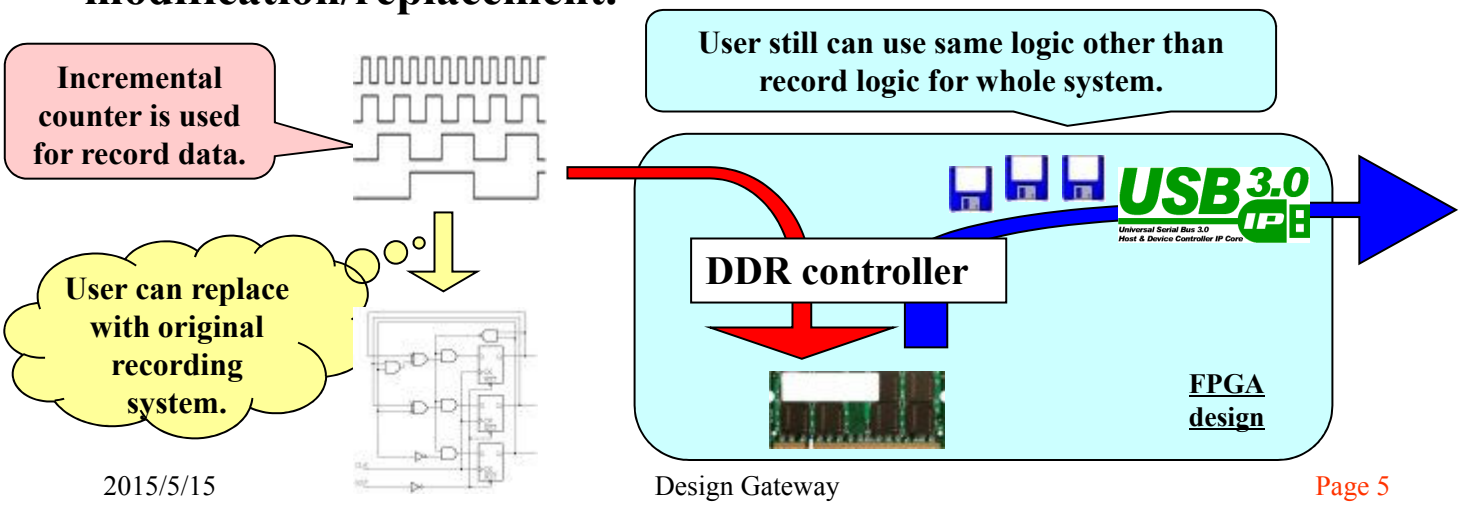
System Operation

- Record data by FPGA and store in on-board DDR temporarily.
- Connected PC recognizes data as FAT32 file.
- PC detects record completion file by status file, then read.
- PC reports read operation finish to FPGA via another status file.
- FPGA regards read operation finish file to be disposable space.
- Thus, DDR memory is used like FIFO in 32MB file size unit.

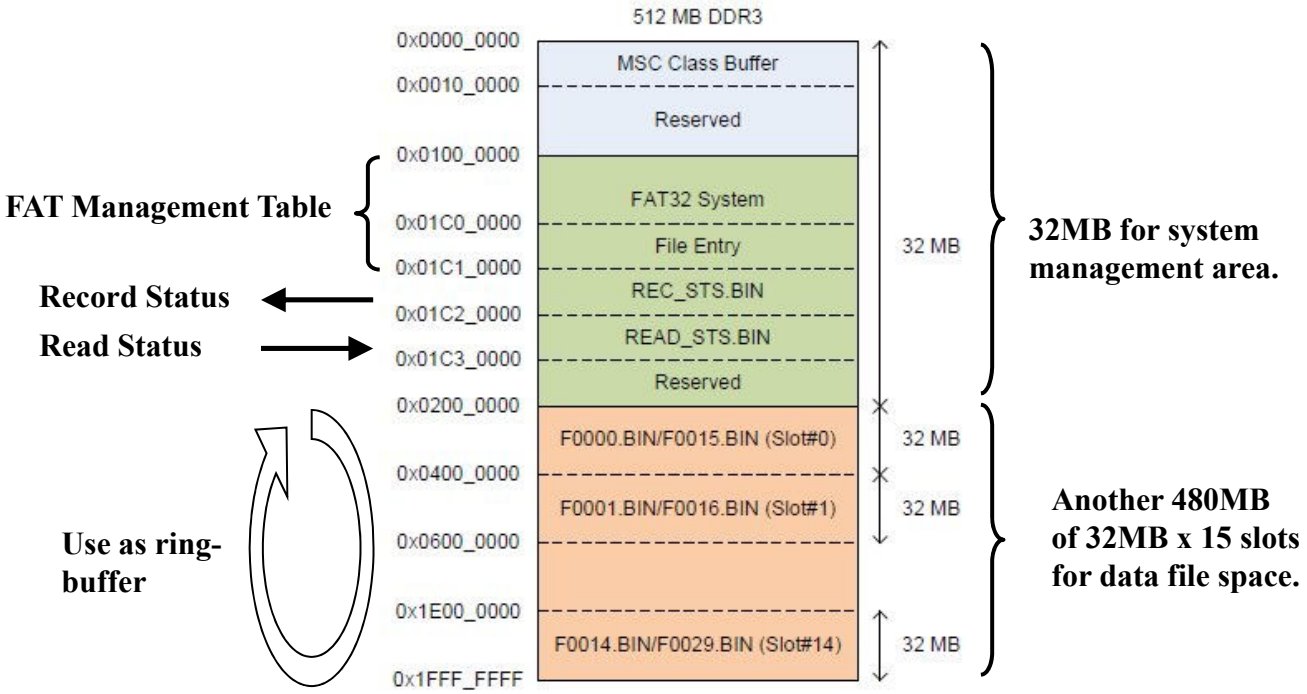


Data Record Operation

- In this reference design, counter data is used for record data.
- It records incremental counter value to DDR memory.
- Sustained record speed is 256MB/sec.
  (User can change record speed by HDL modification)
- User can build original recording system only by record logic modification/replacement.



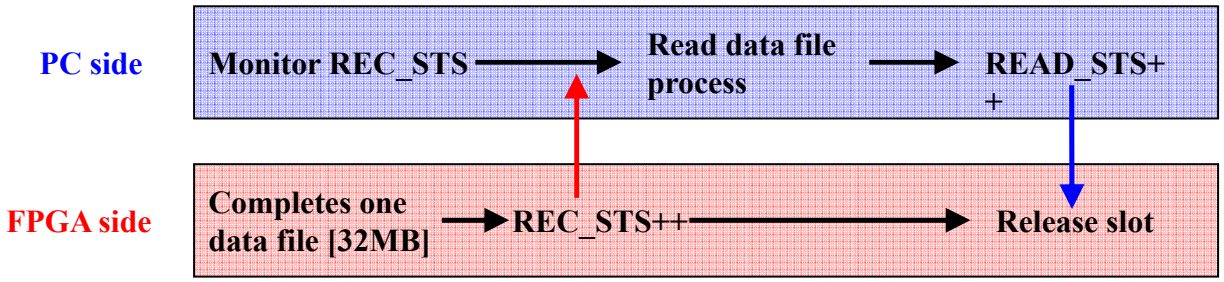
DDR Memory Structure



512MB DDR Memory Map

Buffer Management

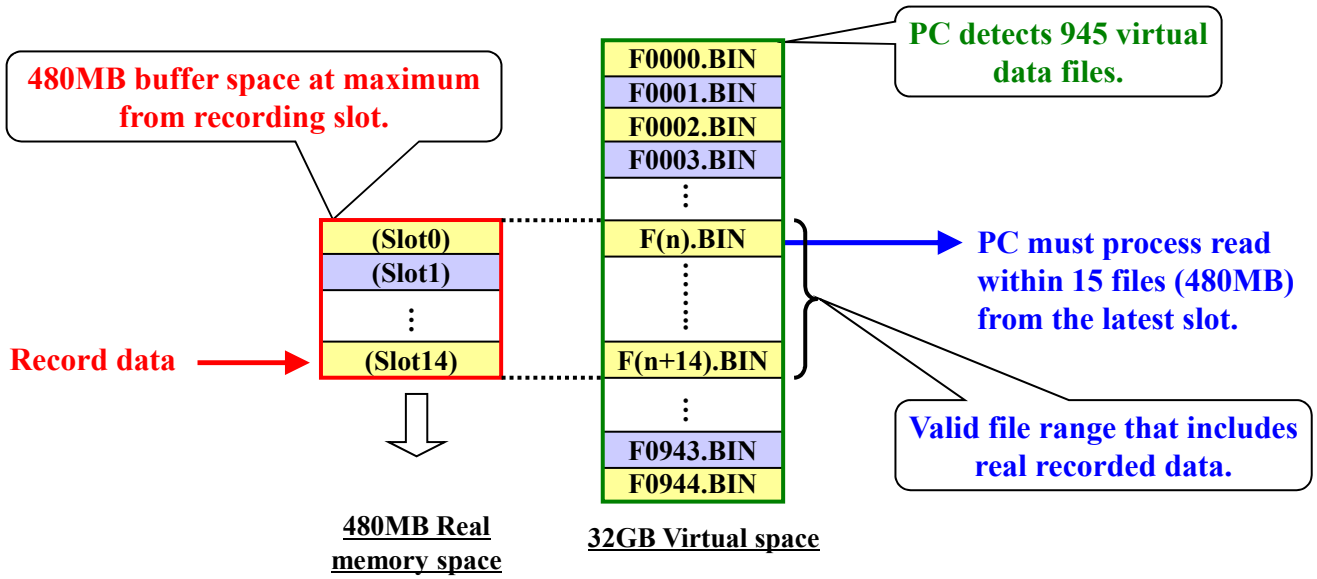
- 32MB recording data completes one data file.
- Then REC_STS (Recording Status) value is incremented.
- PC detects REC_STS update and executes read data file operation, then increments READ_STS (Reading Status).
- FPGA detects READ_STS update and release processed slot.
- When all slots become full, system stops to avoid overflow.



Buffer management flow

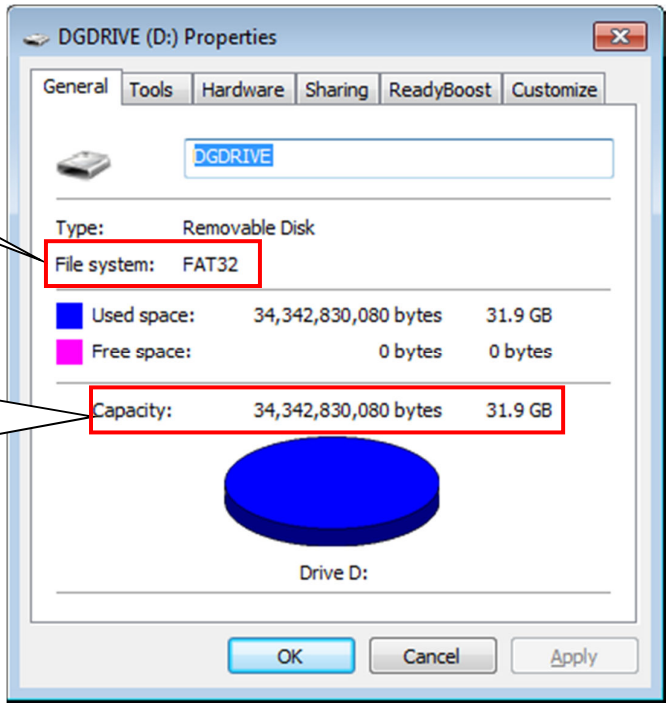
Virtual File Structure

- Expands 480MB real DDR space to 32GB virtual space.



Virtual Space structure

Drive Detection from the PC

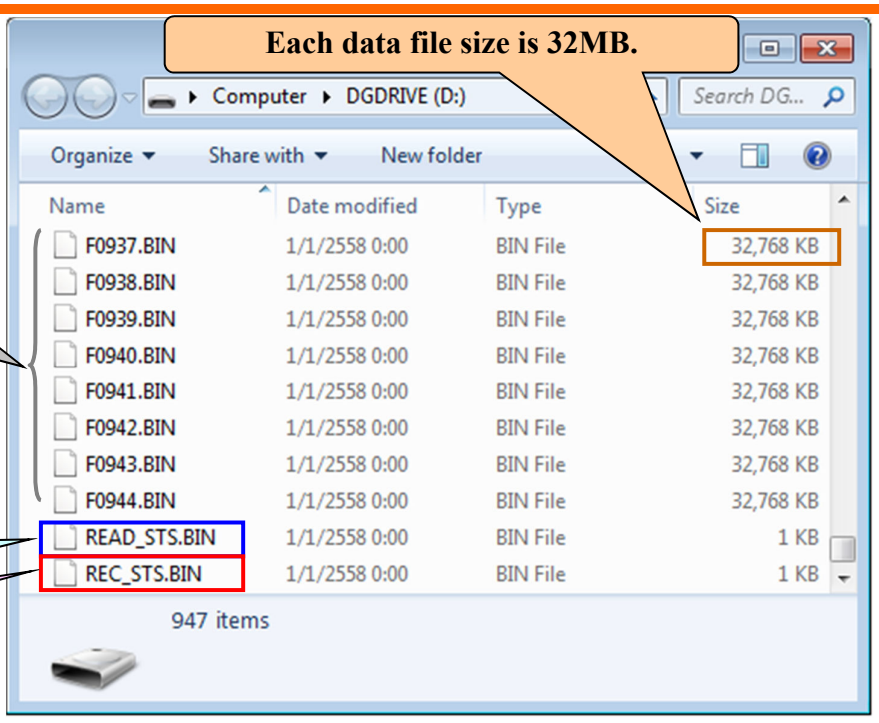


Recognized by the FAT32 format.

Drive Capacity : 32GB
Note) Actual Memory capacity is 32MBx15slot=480MB, so the other space is virtual memory.

Drive properties at the connected PC

File Detection from the PC



945 Data files
Note) Actual data file that includes real data is 15 files at maximum, so the other files are virtual file.

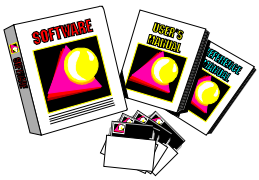
It includes file location information of read process.

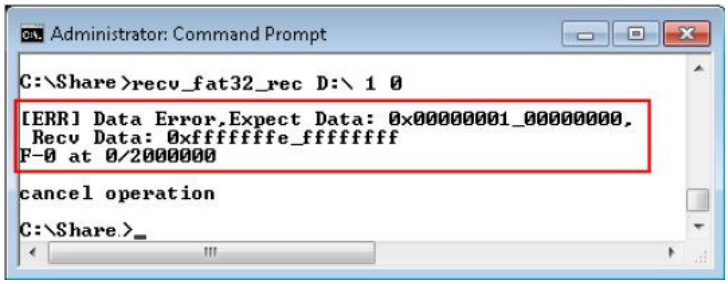
It includes file location information of recorded process.

Folder status at the connected PC

Test Application Software on the PC

- **Test Application**
  - **DOS appication on Windows.**
  - **C-Source code is attached to the reference project.**
- **Software Operation**
  - **Monitors REC_STS to detect new data file at FPGA.**
  - **Executes recorded data, and increments READ_STS after read completion.**
  - **Executes verification with incremental data pattern when verify is specified.**

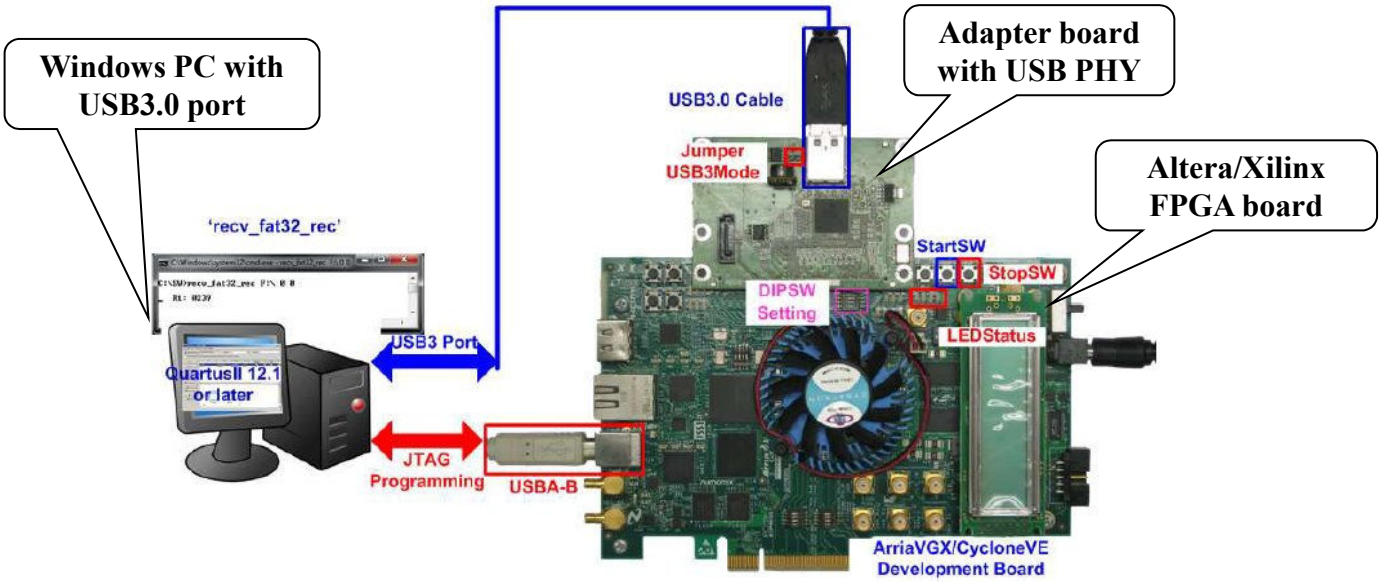




Test Application (Verify error case)

Evaluation Environment

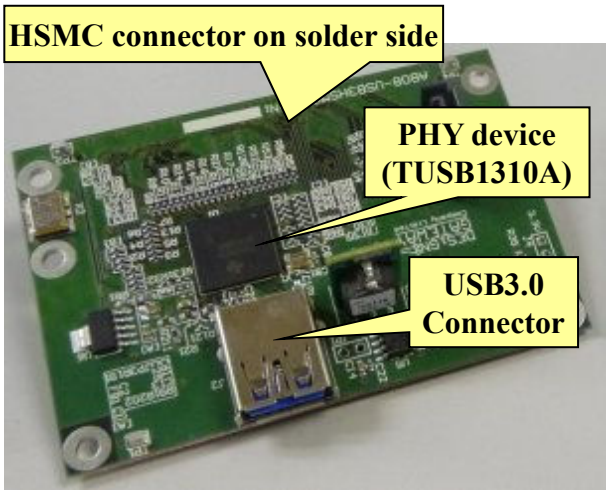
- **Supports standard Altera/Xilinx evaluation FPGA board.**
- **Evaluation sof/bit available before purchase.**



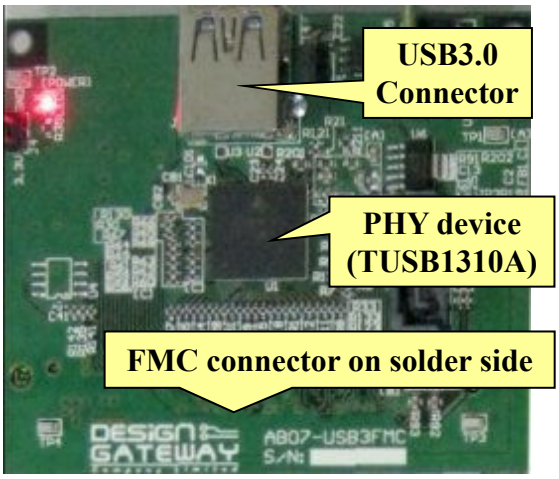
Evaluation Environment for Altera (almost the same for Xilinx)

USB Adapter Board

- FMC (Xilinx) / HSMC (Altera) expansion board.
- Available from DesignGateway.



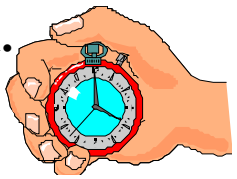
HSMC expansion board for Altera



FMC expansion board for Xilinx

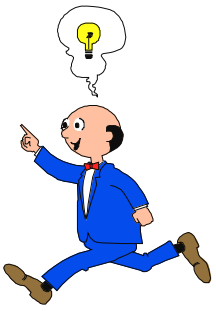
Conclusion

- Versatile Recording System
  - Any OS such as Windows or Linux supports USB3.0 + FAT32
  - Popular fopen() or fread() function available for software development.
- USB3.0 Data Recorder development within short-term.
  - Reference design operation with real board
  - Full source code included except IP-Core
  - Quick prototype development only by recording circuit modification.
  - Check real board operation with evaluation sof/bit file before purchase.



Inquiry

- **Detailed technical document available on website.**
  - **For Altera: http://www.dgway.com/USB3-IP_A_E.html**
  - **For Xilinx: http://www.dgway.com/USB3-IP_X_E.html**
- **Customization**
  - **Customization service available from DesignGateway.**
- **Inquiry**
  - **Design Gateway Co.,Ltd.**
  - **http://www.design-gateway.com/contact.html**
  - **FAX : +66-2-261-2290**



Revision History

Rev.	日時	Description
1.0E	13th-May-201	English Version 1st release