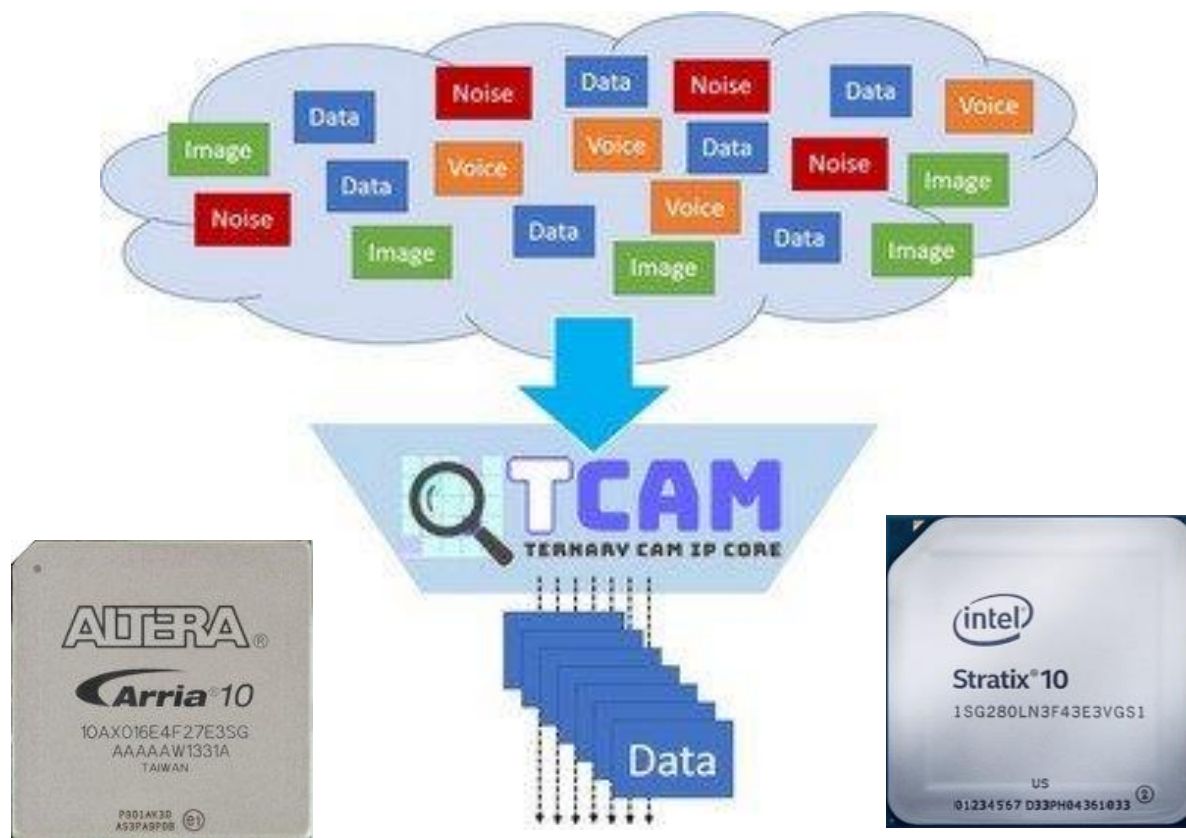


tCAM-IP for Intel introduction

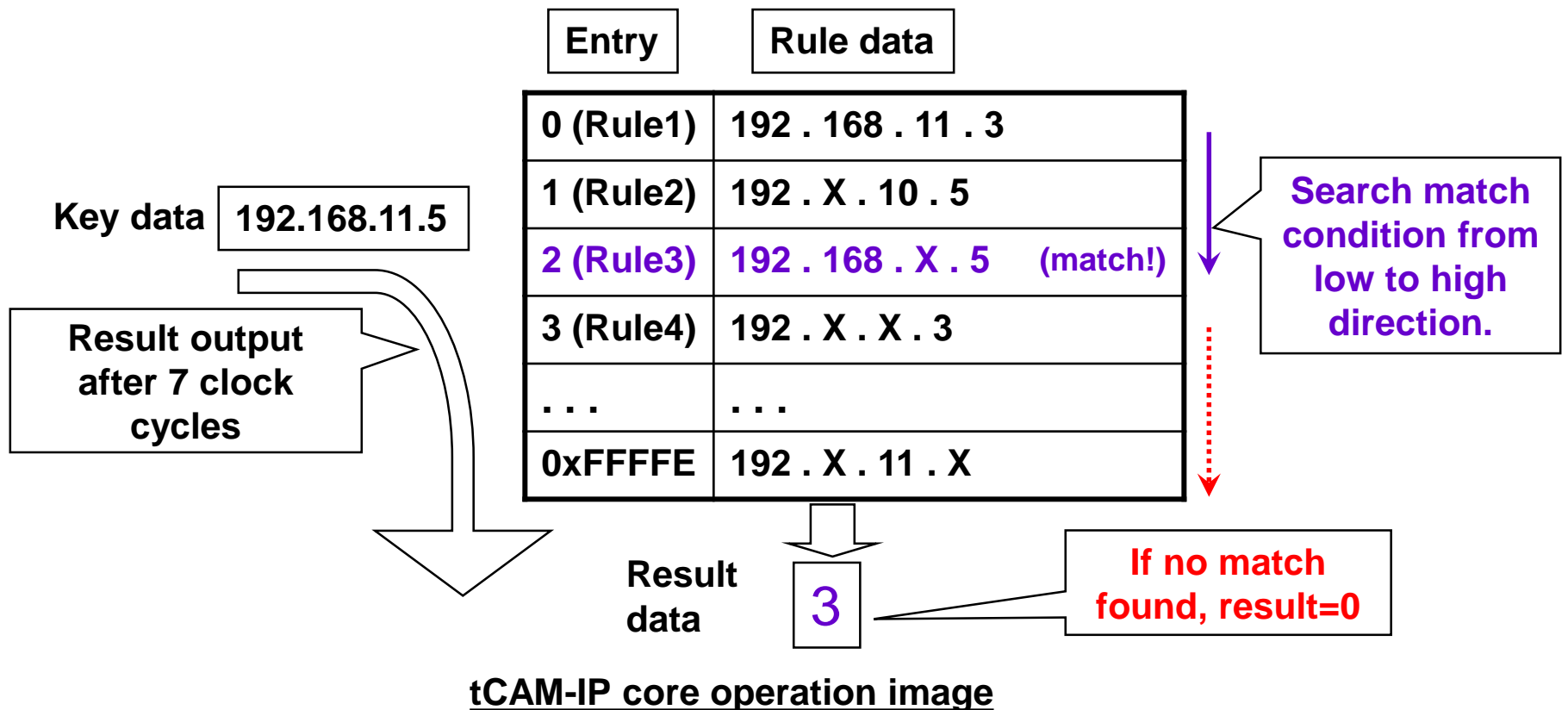
Rev1.0E



Super-low latency Ternary-CAM IP-Core

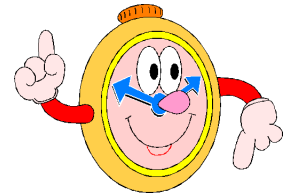
tCAM-IP core summary

- Super low latency ternary (0,1,X) CAM controller IP core.
- Searching latency=7 clock (constant), up to 1M rule entry.



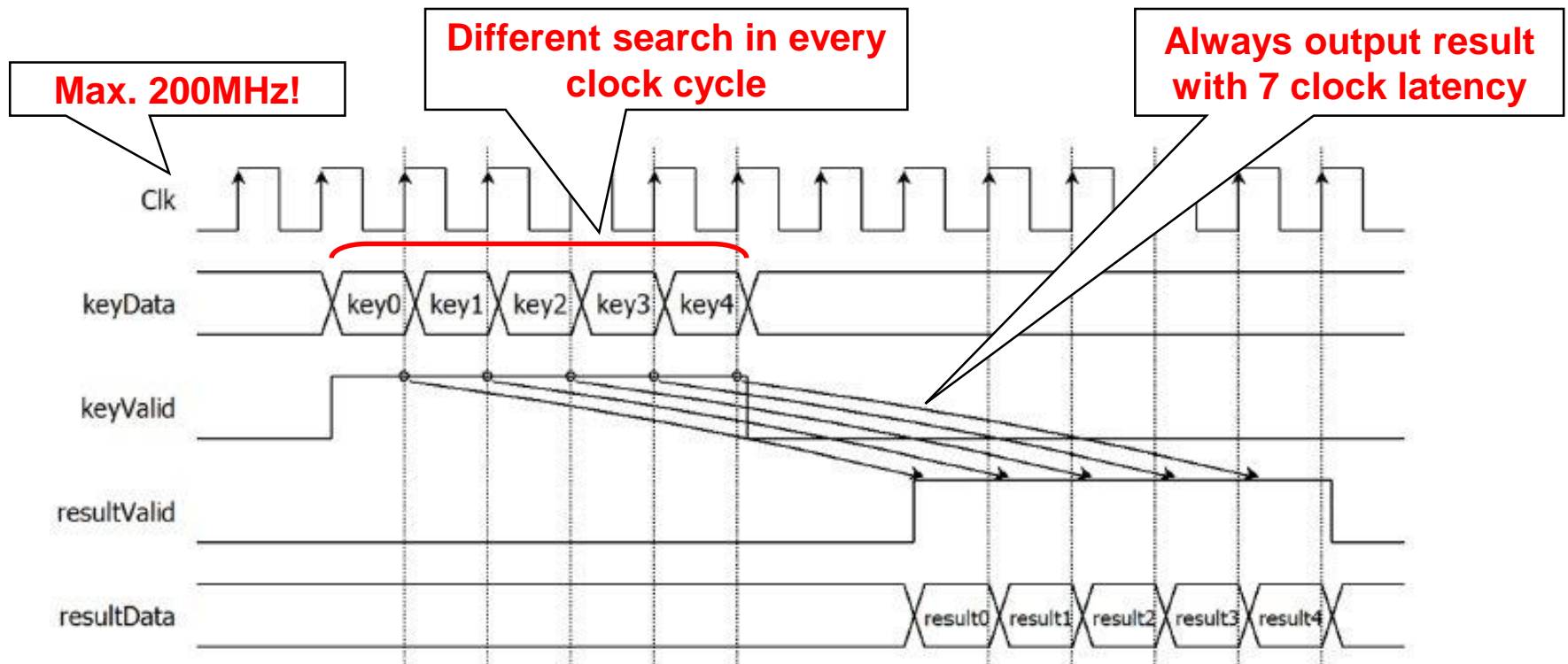
tCAM-IP core advantage

- **Continuous operation under 200MHz clock speed.**
- **Searching latency is constant at 7 clock cycles.**
- **Up to 1M rule entries.**
- **Key bit width 64/56/48/40/32/24 bits**
- **Support customization**
 - Expand rule entry count or key bit width.
 - Support external memory usage.



tCAM-IP core advantage (detail1)

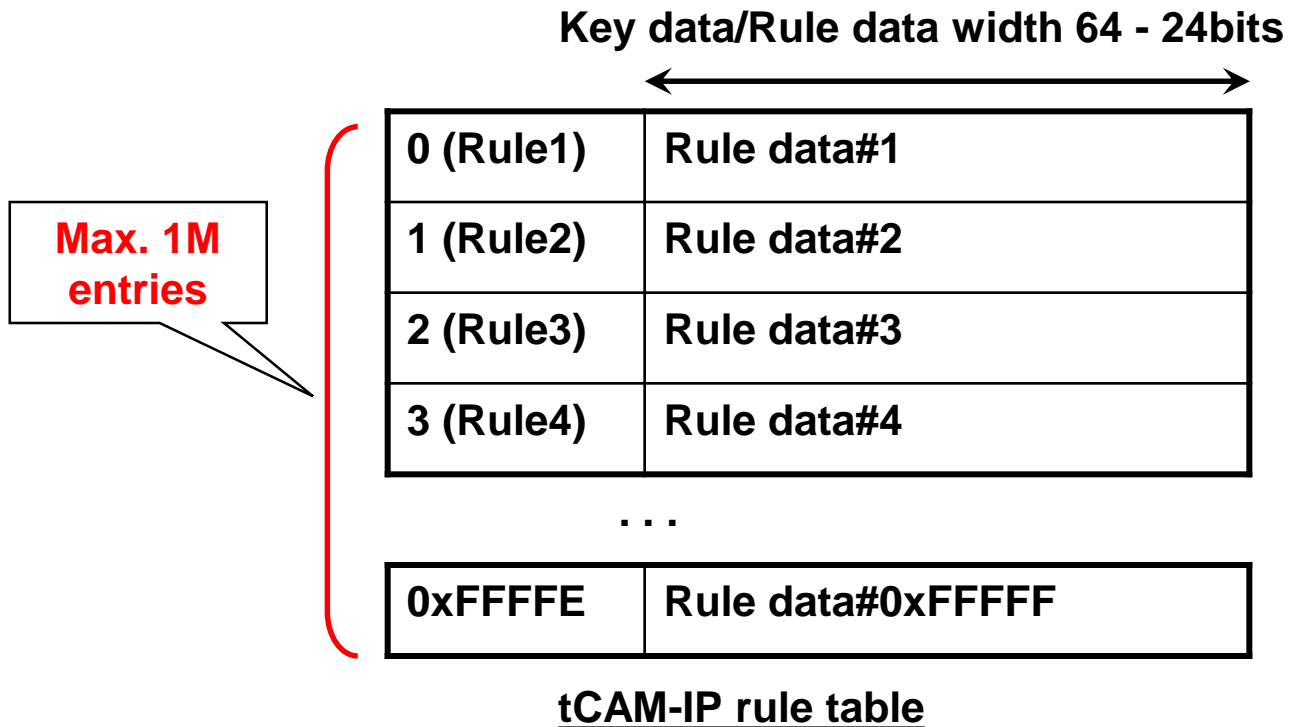
- Searching latency is constant at 7 clock cycles.
- Continuous search operation in every clock (fmax=200MHz).



Timing waveform during search operation

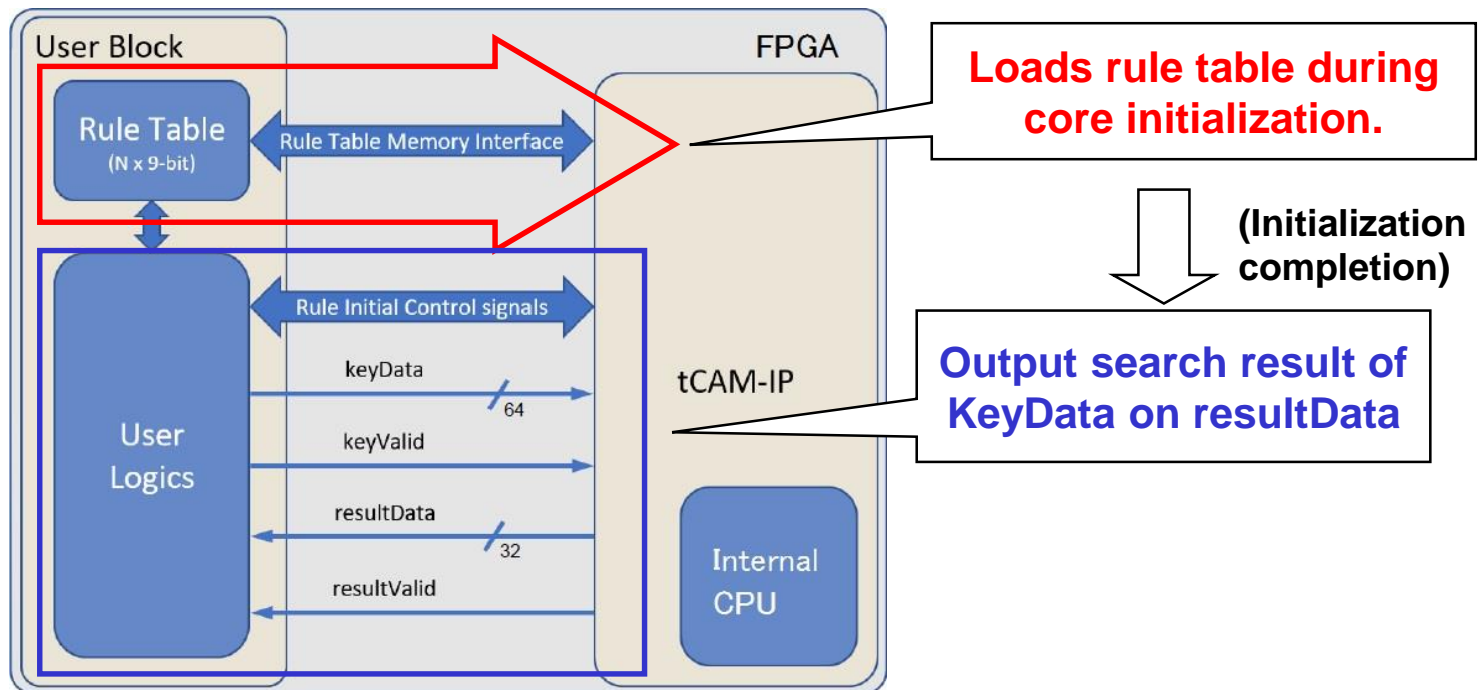
tCAM-IP core advantage (detail2)

- Rule count 1Mega entries at maximum.
- Key data width: Selectable from 64/56/48/40/32/24 bits.



tCAM-IP core operation

- tCAM-IP core loads rule table during initialization.
- Search result of KeyData appears on resultData.



tCAM-IP core operation

tCAM-IP core initialization

- Initialization starts by ruleInit assertion.
- tCAM-IP core loads rule table from user block area.
- tCAM-IP negates ruleBusy after initialization.
- If result status is OK, search operation is ready.
- Initialization time depends on key and rule table size.

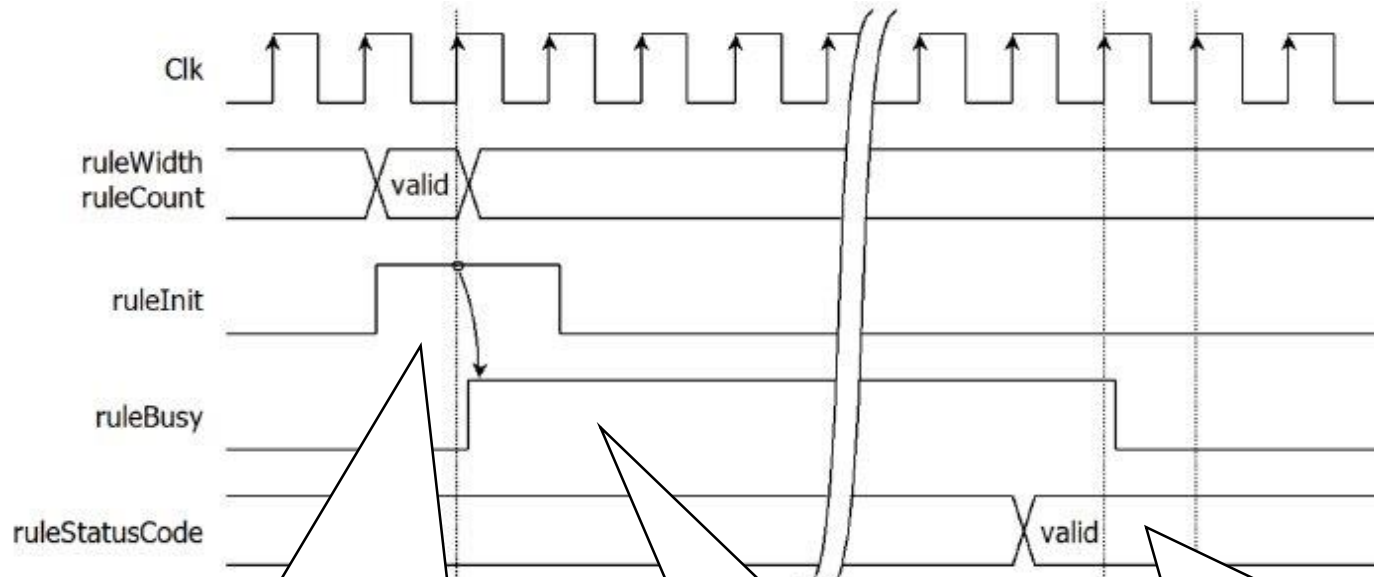
Key width	Rule size	Init. time
32bit	1K	523msec
32bit	64K	2,957msec
64bit	1K	620msec
64bit	64K	15,472msec

tCAM-IP core initialization time



tCAM-IP core initialization (detail1)

- tCAM-IP loads rule data from user block area



User asserts ruleInit together with Key width and rule table size

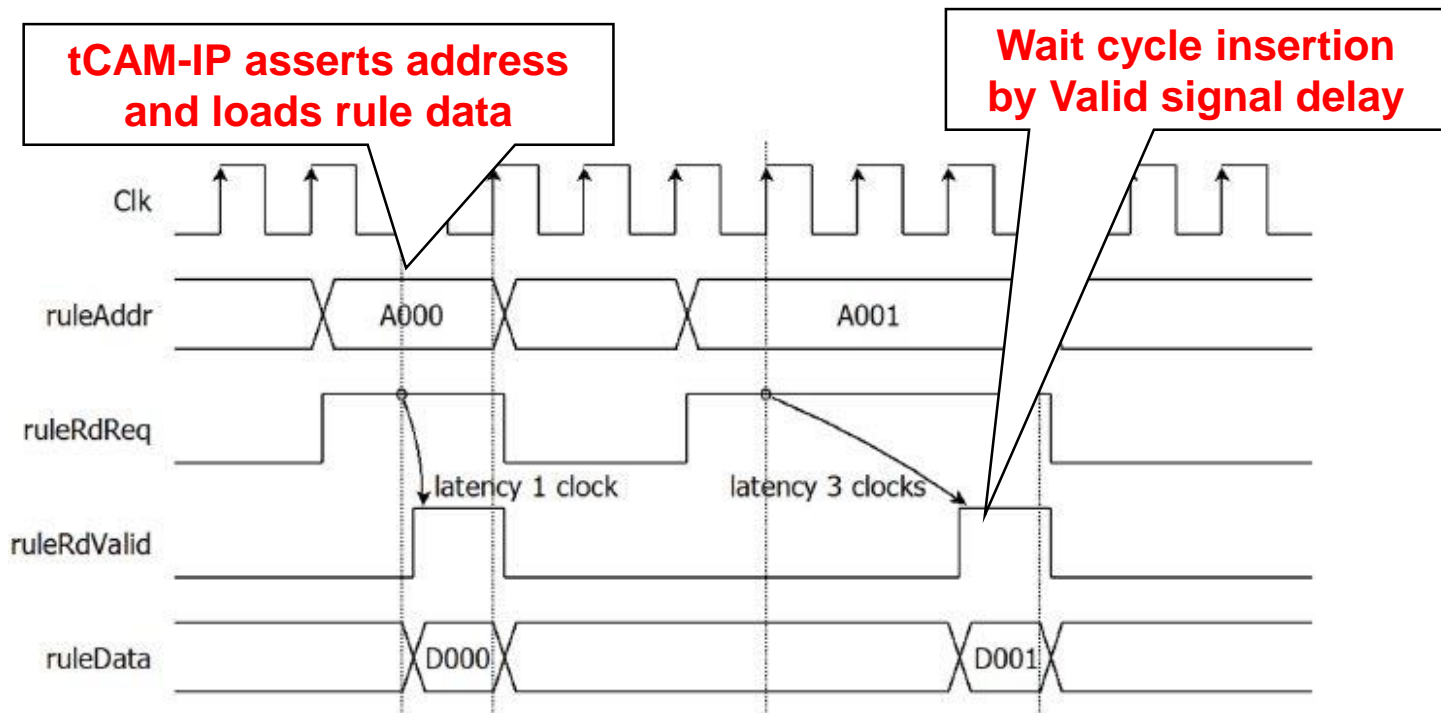
ruleBusy='1' during initialization

User can start operation if result status is OK

tCAM-IP initialization timing waveform

tCAM-IP core initialization (detail2)

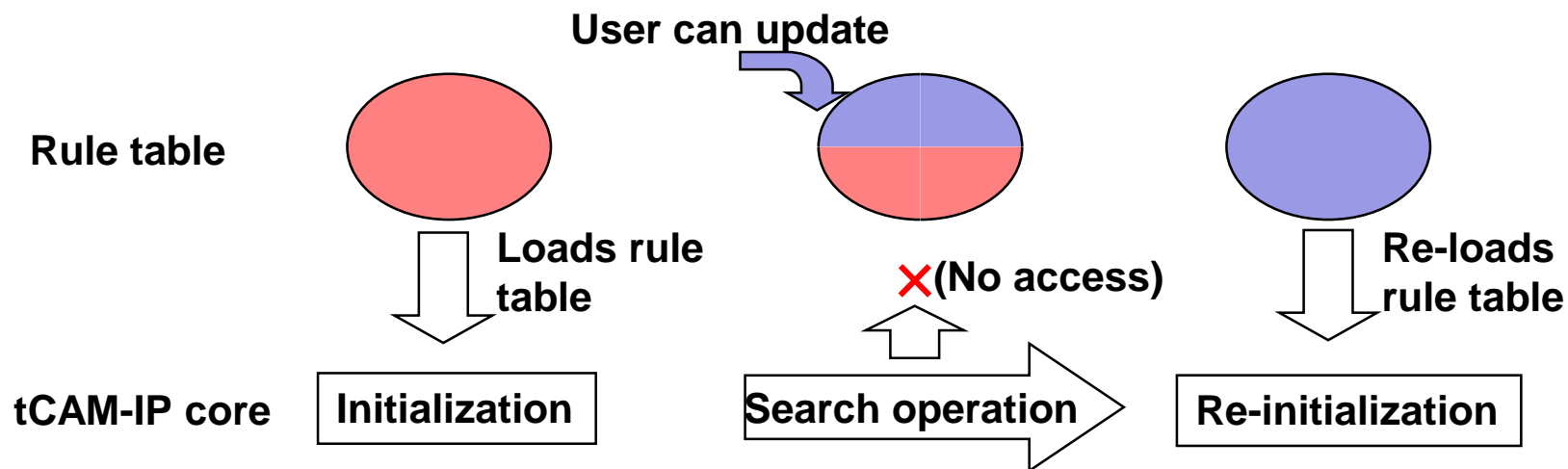
- tCAM-IP loads and scans rule table data in user block.
- User can insert wait cycle by controlling ruleRdValid.



tCAM-IP core rule data access timing waveform

Rule table update

- tCAM-IP does not access to rule table after initialization.
- User can update rule data during core operation.
- tCAM-IP re-loads updated data by re-initialization.



Rule table update during search operation

Resource usage

- Resource usage of FPGA fabric and block memory

Table 1: Example Implementation Statistics for tCAMIP 64-bit up to 1M rule entries

Family	Example Device	Fmax (MHz)	ALMs	Registers ⁽¹⁾	M20Ks ⁽²⁾	Design Tools
Arria10 SX	10AS066N3F40E2SGE2	200	3,042.5	2,710	1,328	QuartusII 16.0

Table 2: Example Implementation Statistics for tCAMIP 32-bit up to 512K rule entries

Family	Example Device	Fmax (MHz)	ALMs	Registers ⁽¹⁾	M20Ks ⁽²⁾	Design Tools
Arria10 SX	10AS066N3F40E2SGE2	200	1,782	2,219	652	QuartusII 16.0

Notes:

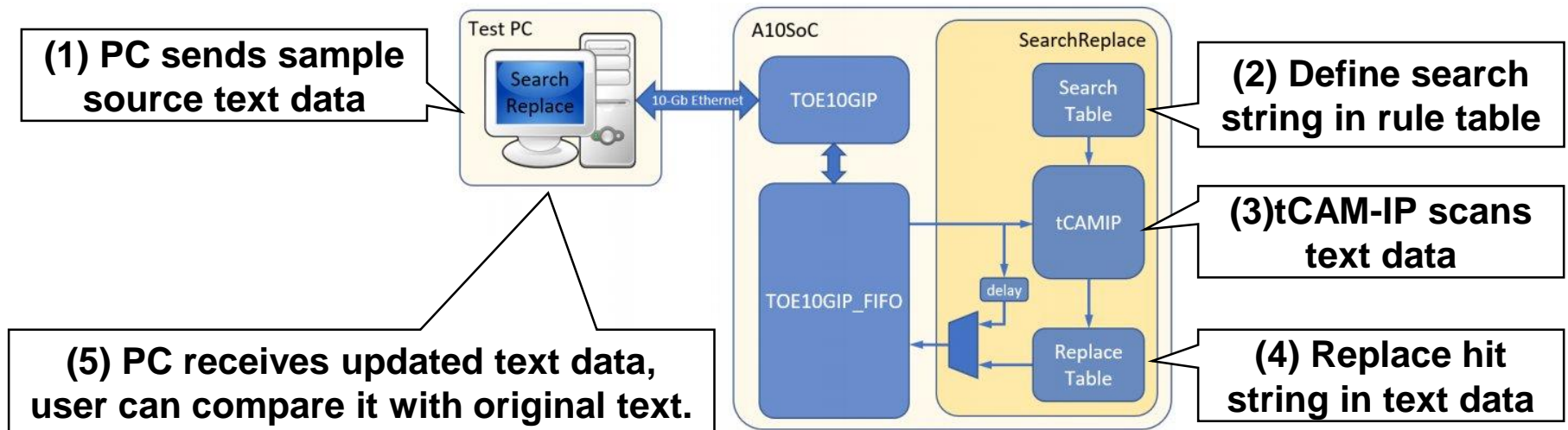
(1) Actual logic resource dependent on percentage of unrelated logic.

(2) Exclude user rule table memory, Ex: 512K x 9-bit rule table memory will take 288 M20Ks.

tCAM-IP core resource usage

Demo1 (Search&Replace demo)

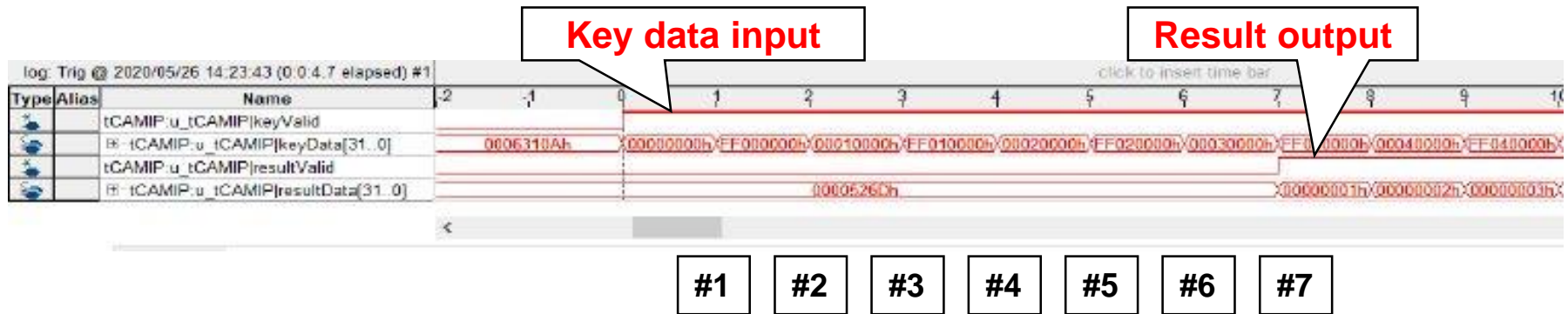
- Connect PC and Arria10SX by 10GbE.
- PC sends sample source text data to FPGA.
- tCAM-IP core searches specified string in text data, then replace it with another string.
- PC receives updated text data after replacement.



tCAM-IP core search and replace demo

Demo2 (SignalTAP waveform)

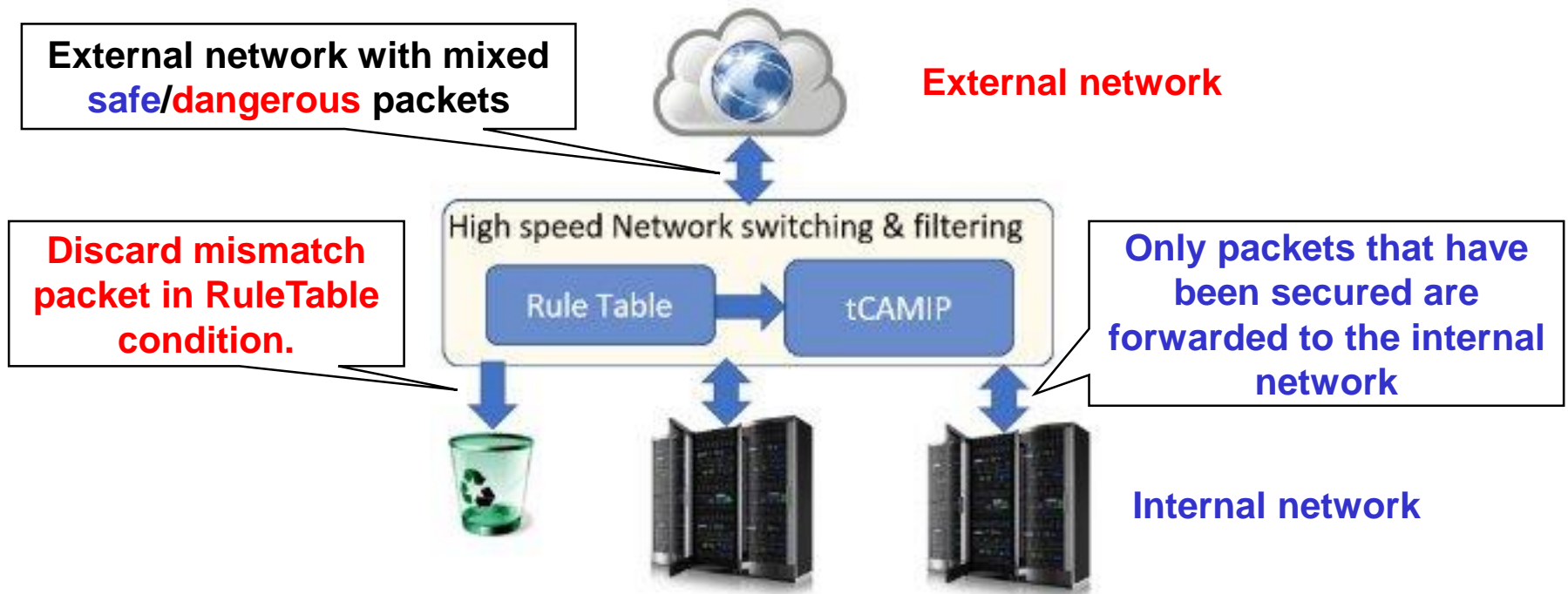
- Measure real search time by SignalTAP.
- System clock frequency = 200MHz.
- User can confirm 7 clocks latency search time.



tCAM-IP waveform measured by SignalTAP

Application example

- Network switch or filtering system.



Network security system by tCAM-IP

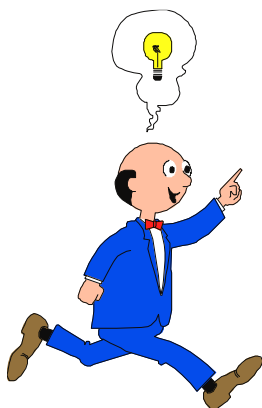
For more detail

- Detailed technical information available on the web site.

https://dgway.com/tCAM-IP_A_E.html

- Contact

- Design Gateway Co.,. Ltd.
- sales@design-gateway.com
- FAX: +66-2-261-2290




The screenshot shows the Design Gateway website for the tCAM IP core. The page features a navigation menu with links for TOP NEWS, GIGA BIT IP CORES (Storage & Network IP), Application Specific IP (For Fintech), SERVICE (Technology&Service), and ABOUT COMPANY. The main content area highlights the tCAM IP core's performance: 200 MSPS By-Constant Latency At-7 Clock Cycles. A detailed description states that tCAM-IP is a high-performance, low-latency, and highly configurable ternary content-addressable memory IP. It can make deterministic search at 200MSPS continuously speed with constant latency at 7 clock cycles. It can achieve matching/filtering performance at 200,000,000 packets per second over 40G/100G Ethernet. It is ideal for various applications such as network packet filtering/forwarding, intelligent switch/router, deep packet inspection and network security application. The page also lists features such as key width (64/56/48/40/32/24/16 bits), up to 1M rule entries, constant searching latency at 7 clock cycles, and a simple rule table memory setup and user interface signals. A diagram on the right illustrates the 'Super High-speed Searching & Filtering' process, showing data packets being processed by the tCAM IP core.

