

# tCAM-IP Demo Instruction

Rev1.0 1-Jul-20

This document describes the instruction to demonstrate the operation of tCAM-IP on Arria10SoC development boar. This demonstration uses tCAM-IP demo software to communicate with development board via 1-Gb Ethernet for preparing rule table, initializing tCAMP-IP, sending keys and reading result data. User is also able to use SignalTap to see the operation of provided signal in FPGA.

# 1 Environment Setup

To operate tCAM-IP demo, please prepare following test environment.

- 1) FPGA development boards (Arria10SoC development board)
- 2) Test PC with 1-Gb Ethernet connection.
- 3) Micro USB cable for JTAG connection connecting between FPGA development board and PC
- 4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA development board and PC
- 5) Quartus Prime for programming FPGA, installed on Test PC
- 6) File "tCAMIPDemoPack.zip" that included Test Application named "tCAM-IP Demo", configuration file named "tCAMIPTest\_time\_limited.sof" and SignalTap file named "stp1.stp".

(to download this file, please visit our web site at www.design-gateway.com)

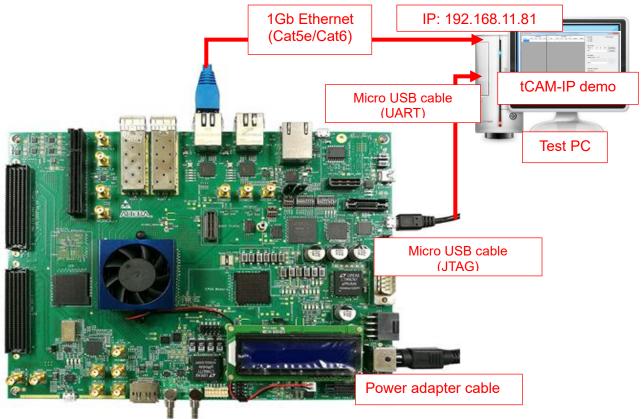


Figure 1-1 tCAM-IP demo (FPGA<->PC) on Arria10SoC board



# 2 PC Setup

Before running demo, please check the network setting on PC. Ethernet setting is shown as follows.

Network and Sharing Center		
🗧 🔶 👻 🛧 🕎 > Control Pane	el > Network and Internet > Network and Sh	aring Center ・ つ Search C
Control Panel Home	View your basic network informati	on and set up connections
Change adapter settings	View your active networks	
Change advanced sharing settings	<b>Network</b> Public network	Access type: Internet 2 Connections: <u>Ethernet</u>
	Change your networking settings	
	Figure 2-1 IPv4 setting	

- 1) Open Ethernet setting option from Control Panel -> Network and Internet -> Network and Sharing Center.
- 2) Click Ethernet icon which is used to connect with FPGA board.

📱 Ethernet Status	× Ethernet Prop	erties X
General	Networking	
Connection IPv4 Connectivity: No Internet access IPv6 Connectivity: No network access Media State: Enabled Duration: 01:56:55 Speed: 1.0 Gbps Details	This connection of Client for Client for	1-Gb LAN connection memet Connection (7) 1219-V Configure uses the following items: r Microsoft Networks Printer Sharing for Microsoft Networks cket Scheduler Protocol Version 4 (TCP/IPV4) ft Network Adapter Multiplexor Protocol ft LLDP Protocol Driver
Activity Sent — Received Bytes: 39,299,554 503,073,087	Install Description Transmission O wide area netv	Protocol Version 6 (TCP/IPv6) Uninstall Properties Control Protocol/Internet Protocol. The default work protocol that provides communication interconnected networks.
Clos		OK Cancel

Figure 2-2 Select IP address setting menu

- 3) Click Properties button in Ethernet Status window.
- 4) Select "TCP/IPv4".
- 5) Click Properties button in Ethernet Properties window.



 $\times$ 

Internet Protocol Version 4 (TCP/IPv4) Properties

General	
You can get IP settings assigned auton this capability. Otherwise, you need to for the appropriate IP settings.	
Obtain an IP address automatical	у
• Use the following IP address:	6a
IP address:	192 . 168 . 11 . 81
Subnet mask:	255 . 255 . 255 . 0
Default gateway:	
Obtain DNS server address autom	natically
• Use the following DNS server add	resses:
Preferred DNS server:	
Alternate DNS server:	
Validate settings upon exit	Advanced
	OK Cancel

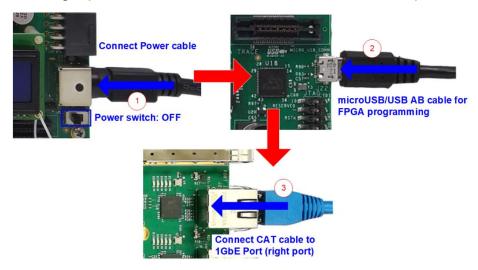
Figure 2-3 Set IP address

6) Set IP address = 192.168.11.81 and Subnet mask = 255.255.255.0. After that, click OK button to confirm IP address setting.



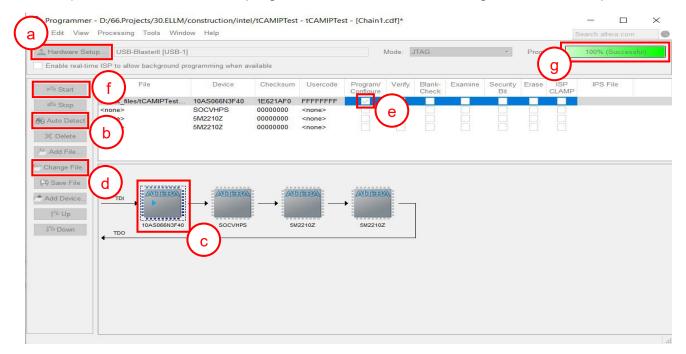
# 3 FPGA board setup

- 1) Make sure power switch is off and connect power supply to FPGA development board.
- 2) Connect USB cable between FPGA board and PC via micro USB
- 3) Connect CAT5e/CAT6 cable between PC and Ethernet connection of FPGA board. User must use the right port when FPGA board has two 1Gb Ethernet ports.



#### Figure 3-1 Power, Ethernet, and micro USB cable connection

- 4) Power on system.
- 5) Open QuartusII Programmer to program FPGA through USB-1 by following step.
  - a) Click "Hardware Setup..." to select USB-BlasterII [USB-1].
  - b) Click "Auto Detect" and select FPGA device. (10AS066N3).
  - c) Select FPGA device icon.
  - d) Click "Change File" button, select SOF file in pop-up window, and click "open" button
  - e) Check "program"
  - f) Click "Start" button to program FPGA and wait until Progress status is equal to 100%



# Figure 3-2 FPGA Programmer



- 6) When configuration is completed, user can check status LEDs on board as Figure 3-3
  - LED#1 is always blink to show clock is working.
  - LED#2 is tcamRstB signal. This LED#2 is related to hardware reset switch "S10".
  - LED#3 is "Connection on" status of TOE1G-IP. This LED is on when software open connection to board.
  - LED#4 is "Ready" status of TOE1G-IP. This LED is on when ethernet connection between PC and board is ready.

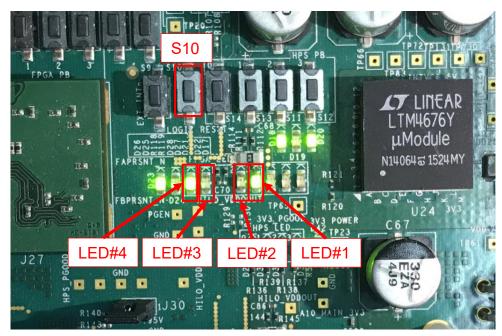


Figure 3-3 LEDs status on board



# 4 SignalTap setup

This designed block diagram of this demo is shown as in Figure 4-1. SignalTap is prepared to see all control signals between tCAM-IP and user logics design.

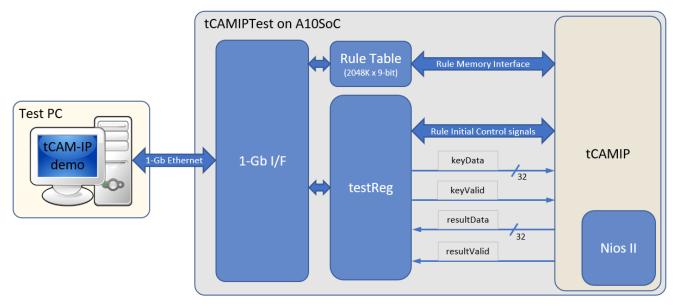


Figure 4-1 Demo environment block diagram

#### 4.1 SignalTap operations

Step to use SignalTap II Logic Analyzer is as follows.

- a) Click File -> Open ..., then select file type to SignalTap II Logic Analyzer Files (\*.stp)
- b) Select "stp1.stp", then click Open button as shown in Figure 4-2
- c) As in Figure 4-3, connect FPGA board by select Hardware to USB-BlasterII.
- d) Setup trigger condition to specify signals behavior. Sample of trigger condition and result is shown as in topic 4.2
- e) Click "Run Analysis" button, wait to capture signals from tCAM-IP.
- f) The result will be shown, when do SignalTap detect signals same as trigger condition.



	Open File				×
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asks	Organize  New folder  66.Projects  69.Projects-Backup  WillLoad  Downloads  Google Drive  cheats  datasheet  Desktop  states	Name A sysec db increme ip output softwar r stp1.stp v <	ental_db 5/22/2 files 5/25/2 5/22/2 e 5/22/2	Project Files (*.qpf) Quartus Prime Archive I Quartus Prime Design T Other Source Files (*.gdf 4 bo Signal Tap II Logic Anal Di Variation Files (*.gdf 4 bo Signal Tap II Logic Anal Di Variation Files (*.gdf In-System Sources and State Machine Editor File Test Bench Output Files Memory Files (*.mif *.ht Programming Files (*.cd *.script Files (*.tcl *.scc *.	Template Files (*.par) c *.v *.vlg *.vh *.verilog *.pkg *.bs df *.bef *.sym) yzer Files (*.stp) ~.qsys *.stp *.ip) e Files (*.lai) Probes Files (*.spf) iles (*.smf) s (*.vht *.vt) ex) df *.sof *.pof *.jam *.jbc *.jic *.jcf
>	0	pen as:			vo *.vho *.tdo *.sdo *.tao *.pin)
All	File name:	stp1.stp	a	SignalTap II Logic Anal	Cancel

# Figure 4-2 Open file "stp1.stp"

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🕄 au	0 0	Not running	$\checkmark$	1183 cells	16896 bits	0 blocks	2 blocks	0 blocks						•	-	
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(																1
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	tCAMIP:u_tCAM				_											
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	tCAMIP:u_tCAM				_											
	_ ⊞-tCAMIP:u_tC	CAMIP resultData[3	10]			000052	6Dh			X <u>000000</u>	<u>01hX00000</u>	002hX000000	<u>103hX000001</u>	<u> 304hX00000</u>	005h)(00000006h	X0000000262
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🔝 auto_s	signaltap_0															
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# Figure 4-3 SignalTap II Logic Analyzer



#### 4.2 SignalTap trigger condition

On demo running, user is able to use SignalTap to setup trigger condition and check the signal waveform after trigger is detected. The prepared SignalTap signals are separated to 3 parts as (1) Rule Initial control signals, (2) Rule Memory interface signals and (3) Input keys & search result signal respectively.

#### 4.2.1 To see Rule Initial Control signals

Figure 4-4 show trigger condition and Figure 4-5 show sample result from SignalTap when user do initial rule table in topic 0

trigge	er: 20	20/05/27 16:23:21 #0	Lock mode:	子 Allow all ch	anges
		Node	Data Enable	Trigger Enable	rigger Conditions
Type /	\lias	Name	186	186	1 🔽 Basic AND ▼
5			$\checkmark$	$\checkmark$	XXXXh
<b>1</b>			$\checkmark$	$\checkmark$	XXXXXXXXh
*		tCAMIP:u_tCAMIP ruleInit	✓	$\checkmark$	1
*		tCAMIP:u_tCAMIP ruleBusy	$\checkmark$	$\checkmark$	
5			$\checkmark$	$\checkmark$	XXXXXXXXh
*		tCAMIP:u_tCAMIP ruleRdReq		$\checkmark$	
*		tCAMIP:u_tCAMIP ruleRdValid		$\checkmark$	
5		tCAMIP:u_tCAMIP ruleData[310]		$\checkmark$	XXXXXXXXXh
5				$\checkmark$	Xh
*		tCAMIP:u_tCAMIP keyValid	~	$\checkmark$	
5		tCAMIP:u_tCAMIP keyData[310]	~	$\checkmark$	XXXXXXXX
*		tCAMIP:u_tCAMIP resultValid	~	$\checkmark$	
5				$\checkmark$	XXXXXXXXXh

#### Figure 4-4 Trigger setup for rule initial control signals

SignalTap II Logic Analyzer - D:/66.Projects/30.ELLM/constructio	nn/intel/tCAMIPTest - tCAMIPTest - [stp1.stp]* - 🗆 🗙	
<u>File Edit View Project Processing Tools Window H</u> elp	Search altera.com	6
🗐 🛃 🤈 (*) 🞋 🔲 🕨 🈫 🚱		
Instance Manager: 🍡 🔊 🔳 🔄 Ready to acquire	× JTAG Chain Configuration: JTAG ready	×
Instance Status Enabled LEs: 2605	Memory: 19046 Small: 0/18520( Medium: 10/21) Large: 0/0	
auto signaltap 0 Not running 2605 cells	Memory: 1946 Small: 0/15/2/L Large: 0/0 Hardware: USB-Blasteril [USB-1]	
	Device: @1: 10AS066H(1 2 2ES)3)3E2[3 V Scan Chair	n
	>> SOF Manager: 🛓 🕴	••
log: Trig @ 2020/05/29 07:07:20 (0:0:11.2 elapsed)	click to insert time bar	
Type Alias Name	649481620242832364044485256	
E::tCAMIP:u_tCAMIP[ruleWidth[150]	0020h	11
tCAMIP:u_tCAMIP[ruleCount[310]	000779DFh	11
tCAMIP:u_tCAMIP ruleInit		
tCAMIP:u_tCAMIP[ruleBusy           ::::::::::::::::::::::::::::::::::::		
	001DE77Bh	211
tCAMIP:u_tCAMIP ruleRdReq		
tCAMIP:u_tCAMIP[ruleRdValid           ::tCAMIP:u_tCAMIP[ruleData[310]		
TCAMIP:u_tCAMIP[ruleData[310]	0000000h	211
tCAMIP:u_tCAMIP ruleStatusCode[30]	1h	211
tCAMIP:u_tCAMIP[keyValid		.
TCAMIP:u_tCAMIP[keyData[310]	1h 0000000h	211
tCAMIP:u_tCAMIP(resultValid		
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	<	
🔁 Data 🛛 🐺 Setup		
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Hierarchy Display: × Data Log: 🛐	×	¢
✓ ✓ ► tCAMIPTest     ✓ ▲ tCAMIP.u_tCAMIP		
auto_signaltap_0		
	0% 00:00:00	

#### Figure 4-5 Sample result for rule initial control signals



#### 4.2.2 To see Rule Memory Interface signals

Figure 4-6 show trigger condition and Figure 4-7 show sample result from SignalTap when user do initial rule table in topic 0

trigge	er: 20	20/05/29 07:09:41 #0	Lock mode:	💣 Allow all ch	anges
		Node	Data Enable	Trigger Enable	rigger Condition
Type /	Alias	Name	186	186	1 🔽 Basic AND ▼
5			$\checkmark$	$\checkmark$	XXXXh
5		tCAMIP:u_tCAMIP ruleCount[310]	$\checkmark$	$\checkmark$	XXXXXXXXh
*		tCAMIP:u_tCAMIP ruleInit	$\checkmark$	$\checkmark$	
*		tCAMIP:u_tCAMIP ruleBusy	$\checkmark$	$\checkmark$	
5		tCAMIP:u_tCAMIP ruleAddr[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh
*		tCAMIP:u_tCAMIP ruleRdReq	✓	✓	1
*		tCAMIP:u_tCAMIP ruleRdValid	$\checkmark$	$\checkmark$	
5		tCAMIP:u_tCAMIP ruleData[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh
5		tCAMIP:u_tCAMIP ruleStatusCode[30]	$\checkmark$	$\checkmark$	Xh
*		tCAMIP:u_tCAMIP keyValid	$\checkmark$	$\checkmark$	
5		tCAMIP:u_tCAMIP keyData[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh
*		tCAMIP:u_tCAMIP resultValid	$\checkmark$	$\checkmark$	
5				$\checkmark$	XXXXXXXXXXh

### Figure 4-6 Trigger setup for rule memory signals

📌 SignalTap II Logic Ana	alyzer - D:/66.Proje	ects/30.ELLM	M/constructio	on/intel/tCAMIP	Test - tCAMIPTe	st - [stp1.stp]	*											-	$\Box$ ×
File Edit View Project	Processing Tools	s Window	Help														[	Search alter	a.com 🌖
🖷   見   つ で   幣 🐽	► 😫 😮																		
Instance Manager: 🍡 👂	🔳 🎦 Ready	to acquire												× J	TAG Chair	n Configurati	ion: JTAG re	eady	×
Instance	Status	Enabled	LEs: 2605	Memory: 1904	6 Small: 0/18520	( Medium: 10/	/213 Large: 0	)/0							lardwara:	USB-Blaste	di IUSB-11	<b>.</b>	Setup
🔝 auto_signaltap_0	Not running	$\checkmark$	2605 cells	190464 bits	0 blocks	10 blocks	0 blocks	6											
														0	)evice:	@1: 10AS0	166H(1 2 2ES	3 3E2 3 -	Scan Chain
														[	>> SOF	Manager:	i. O		
log: Trig @ 2020/05/29 07	.00.00 (0.0.12 8 ala									-6-1	to insert time	h							
Type Alias	.02.22 (0.0. 13.8 elap Name			402 404	406	408	410	412	414 .	416	418	400	422	424	426	5 42	18 4	30 4	32 434
E-tCAMIP:u_tC	CAMIP ruleWidth[15.			,	, "I"	448 .	410 .	112	, 11 <sup>,</sup> ,	-10	0020h	440 .	, apr	141	, 440	o , 44	8 , 4	1°, '	42 . 401
	CAMIP ruleCount[31.										000779DFh								
tCAMIP:u_tCAM																			
tCAMIP:u_tCAN											0								
	CAMIP ruleAddr[31	0]			0000000	Dh	X				<u> </u>		00000004h	1					
tCAMIP:u_tCAM												_							
	CAMIP ruleData[31	01									00000000h								
	CAMIP (ruleStatusCo										00000000								
tCAMIP:u_tCAM		00[00]																	
	CAMIP[keyData[31	0]									00000000h								
tCAMIP:u_tCAM	/IP resultValid																		
E-tCAMIP:u_t0	CAMIP resultData[31	0]									00000000h								
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Data 🐺 Setup				`															,
Hierarchy Display:	×	Data Log:	<b>Fa</b>																×
V ✓ → tCAMIPTest V CAMIP:u_tCA		auto_sig																	
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																		07	

#### Figure 4-7 Sample result for rule memory signals



#### 4.2.3 To see Input key and Search result signals

Figure 4-8 show trigger condition and Figure 4-9 show sample result from SignalTap when user do initial rule table in topic 5.6

trigger:	: 2020/05/29 07:09:41 #0		Lock mode:	子 Allow all ch	anges
	Node		Data Enable	Trigger Enable	rigger Conditions
Type Ali	ias Name		186	186	1  Basic AND ▼
5		$\checkmark$	$\checkmark$	XXXXh	
5		$\checkmark$	$\checkmark$	XXXXXXXXh	
*	tCAMIP:u_tCAMIP ruleInit	$\checkmark$	$\checkmark$		
*	tCAMIP:u_tCAMIP ruleBusy	$\checkmark$	$\checkmark$		
5	tCAMIP:u_tCAMIP ruleAddr[310]		$\checkmark$	$\checkmark$	XXXXXXXXh
*	tCAMIP:u_tCAMIP ruleRdReq		$\checkmark$	$\checkmark$	
*	tCAMIP:u_tCAMIP ruleRdValid		$\checkmark$	$\checkmark$	
5			$\checkmark$	$\checkmark$	XXXXXXXXh
<b>a</b>	tCAMIP:u_tCAMIP ruleStatusCode[30]		$\checkmark$	$\checkmark$	Xh
*	tCAMIP:u_tCAMIP keyValid	$\checkmark$	✓	1	
5	tCAMIP:u_tCAMIP keyData[310]	$\checkmark$	$\checkmark$	XXXXXXXXXh	
*	tCAMIP:u_tCAMIP resultValid	$\checkmark$	$\checkmark$		
5			~	$\checkmark$	XXXXXXXXXh

### Figure 4-8 Trigger setup for input key and searching result

% SignalTap II Logic Analy	zer - D:/66.Proje	ects/30.EL	LM/constructio	on/intel/tCAMI	PTest - tCAMIPT	est - [stp1.stp]	*										-	
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Instance	Status	Enabled	LEs: 2605	Memory: 190	46 Small: 0/1852	0( Medium: 10/	/213 Large: 0	/0								terll [USB-1]	-	Cature
🛃 auto_signaltap_0	Not running		2605 cells	190464 bits	0 blocks	10 blocks	0 blocks							Hardware:	USB-Blast	eni (USB-1)	•	Setup
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E tCAMIP:u_tCA										0007	79DFh							
tCAMIP:u_tCAMIF																		
tCAMIP:u_tCAMIP																		
		)]								001D	E77Bh							
tCAMIP:u_tCAMIF																		
tCAMIP:u_tCAMIF				_														
E tCAMIP:u_tCA											0000h							
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#### Figure 4-9 Sample result for input key and searching result



# 5 tCAM-IP demo software

tCAM-IP demo software is used for preparing and sending rule and key pattern data to A10SoC board via 1-Gb Ethernet connection and getting the result of searching from tCAM-IP.

The main features of tCAM-IP demo software are as following.

- 1) Rule creation.
- 2) Key creation.
- 3) Initialization rule data table to FPGA development board.
- 4) Search key data and display result.
- 5) Compare expect data of key data searching to result data of key data searching.

#### 5.1 Demo software interface description

1-IP Demo		
A Rule table No. A+0 A+1 A+2 A+3	b Key data No. A+0 A+1 A+2 A+3 Expect Result	Rule width C tCAM-IP version :
		C Rule Creation Pattern 0 1 2 3 From Pattern File pok\[ELLM]\file Test\test0001.bt From File
		Key Creation     e       Number of key :     0 / 0       Generate from Rule     Stop       File     look\[ELLM]\fileTest\test0001.bd
		Hardware Connection Inital Status : 0 Connect Rule init Search Compare rLatencyCount :

Figure 5-1 Software interface

Figure 5-1 shows tCAM-IP demo software and the description is shown as below.

- a) Rule table is the user rule data display.
- b) Key data table is the user key data display.
- c) Rule width, Users can select data size modes.
- d) Rule Creation, Users can generate rule data table pattern or load rule data table pattern from the file.
- e) Key Creation, Users can generate key data from rule table or load key data table pattern from the file.
- f) Hardware Connection, Users can communicate with FPGA development board in this part. Which consists of connection with board, rule Initialize, key data search, result compare.



#### 5.2 File format for Rule data and Key Data

User can prepare Rule data or Key data file for this demo. The file format is shown as Figure 5-2**Error! Reference source not found.** and Figure 5-3 for rule width 32-bit and 24-bit respectively.

- 1) The first line is header of file for specific number of byte data in this file like "A+0, A+1, A+2, A+3" for 32-bit file format.
- 2) Next lines are data. The valid range of data is 0-255, others number and 'x' is defined to don't care value.

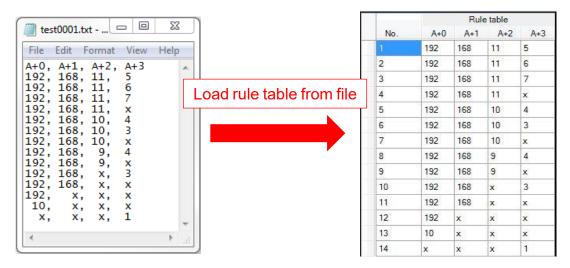


Figure 5-2 Example of load rule file 32-bit



Figure 5-3 Example of load rule file 24-bit



#### 5.3 Rule table creation

To create the rule table, the step is shown as in Figure 5-4.

tCAM-IP D	Jemo													
		Rule	table		[3]			Key	data				Rule width	tCAM-I
No.	A+0	A+1	A+2	A+3		o.	A+0	A+1	A+2	A+3	Expect	Result	🔲 24-bit	
1	x	0	0	0									32-bit	
2	x	0	0	1										
3	x	0	0	2	_								Rule Creation	
4	x	0	0	x	_								Pattern 0 1	2 3 1
5	x	0	1	0	-								File pok\[ELLM]\fileTe	st\test0001.txt
6	x	0	1	1										
7	x	0	1	2	-								Key Creation	
8	x	0	1	x	-								Number of key : 0 / 0	
9 10	x	0	x	0	-								Generate from R	ule Stop
10	x	0	x	2	-								File look \[ELLM]\fileTe	est\test0001.txt
12	x x	0	x x	x	-									
12	x	x	× 0	x 0	-									
14	x	x	0	1									Hardware Connection	
15	×	x	0	2	-								Inital Status: 0	
16	x	x	0	x	-								Connect	Rule init
17	x	x	1	0									Search	Compare
18	x	x	1	1									rLatencyCount :	
19	x	x	1	2										
20	x	x	1	x										
21	x	x	x	0										
22	x	x	x	1										
				2										

Figure 5-4 Rule creation process

- 1) Select Rule width mode for setup data size.
- 2) Create rule table, the user can select 2 modes as follows.
  - i) Generate rule data table from pattern as show in Figure 5-5.
    - a) Fill out valid range (0-256) of each byte in "Pattern". Byte of pattern position starts "A+0" left to right.
    - b) Click "From Pattern" to start generate rule table.

		Rule table				
	No.	A+0	A+1	A+2	A+3	
	1	х	0	0	0	
Generate rule table	2	x	0	0	1	
Rule Creation	3	x	0	0	x	
Pattern 0 1 1 2 From Pattern	4	x	0	x	0	
	5	x	0	x	1	
	6	x	0	x	x	
	7	x	x	0	0	
	8	x	x	0	1	
	9	x	x	0	x	
	10	x	x	x	0	
	11	x	x	x	1	

#### Figure 5-5 Example rule data table pattern.

- ii) Load rule data table from the file by click "From File" button to browse and load rule data file.
- 3) When rule is created, rule data show in rule table as shown in Figure 5-4.



#### 5.4 Key data table creation

🚽 tCAM-IP Demo П X Rule table Key data Rule width tCAM-IP version No A+0 Expect Result No A+0 A+1 A+2 A+3 A+1 A+2 A+3 24-bit ✓ 32-bit х **Rule** Creation x Pattem 250 60 15 1 From Pattern File 1\software\dataTest\test0001.txt From File x i y Creation x Number of key : 53796 / 489952 Generate from Rule Shuffle Key x n\software\dataTest\test0001.txt From File x ii Hardware Connection x Inital Status : 0 Connect x rLatencyCount x x x x

To create key table, the step is shown as in Figure 5-6.

Figure 5-6 Key creation

- 1) Create Key data, the user can select 2 modes as follows
  - i) Generate key data from rule table.
    - a) Click "Generate from Rule" to start generate key data.
    - b) "Number of key: X / Y" is progress status by X is progress number of key and Y is total number of keys from all combination of rules. (generating time depends on the amount of key data)
    - c) "Stop" button is used for stop key generating.
  - ii) Load key data from the file by click "From File" button to browse and load rule data file.
- 2) When key data is created, the expect value will be generated automatically.
- 3) "Shuffle Key" button is used to shuffle each key in key table randomly.



#### 5.5 Initialization rule data to FPGA Development board

The step to initialize rule data is following as below and Figure 5-7.

- 1) Please make sure that LED#4 is on (ready), before click "Connect" button.
- When connection is completed, the text of the button will change to "Disconnect" and LED#3 is turn on (please refer LEDs on board in Figure 3-3). The button "Rule init", "Search" and "Compare" will enable.
- 3) On SignalTap, setup trigger condition when ruleInit = '1' and other signals are don't care. Then press "Run Analysis" button.
- 4) Click "Rule init" button to initialize data of rule table. Initializationi duration time depends on the amount of key data.

"Initial Status: X" is active status for Rule transfer, Rule verify, Rule initial and Status code. By X is running umber of rule table, time count of Rule initial status and status code which shows that process is still running)

- When ruleInit signal = '1', SignalTap will show all interface signals of tCAM-IP.
- In case to see the difference trigger point, user can change trigger condition in SignalTap on step 3).
- 5) When initialization is completed, the message box will popup "Rule initial completed". In case initialization is incompleted, "Initial Status:" is shown error message of status code.

		Rule	e table		^			Key	data				^	Rule width tCAM-IP version :
No.	A+0	A+1	A+2	A+3		No.	A+0	A+1	A+2	A+3	Expect	Result		24-bit
	0	0	0	0		1	0	0	0	0	1			☑ 32-bit
2	0	0	0	×		2	0	0	0	255	2			
3	0	0	1	0		3	0	0	1	0	3			Rule Creation
4	0	0	1	x		4	0	0	1	255	4			Pattern 250 60 15 1 From Patte
5	0	0	2	0		5	0	0	2	0	5			File 1\software\dataTest\test0001.txt From File
6	0	0	2	×		6	0	0	2	255	6			
7	0	0	3	0		7	0	0	3	0	7			Key Creation
8	0	0	3	×		8	0	0	3	255	8			Number of key : 53796 / 489952
9	0	0	4	0		9	0	0	4	0	9			Generate from Rule Stop Shuffle Ke
10	0	0	4	x		10	0	0	4	255	10			
11	0	0	5	0		11	0	0	5	0	11			File n\software\dataTest\test0001.txt From File
12	0	0	5	x		12	0	0	5	255	12			
13	0	0	6	0		13	0	0	6	0	13			Hardware Connection
14	0	0	6	x		14	0	0	6	255	14			Inital Status : 0
15	0	0	7	0		15	0	0	7	0	15		(1	
16	0	0	7	x		16	0	0	7	255	16		$\searrow$	Connect Rule init 4
17	0	0	8	0		17	0	0	8	0	17			Search Compare
18	0	0	8	×		18	0	0	8	255	18			rLatencyCount :
19	0	0	9	0		19	0	0	9	0	19			
20	0	0	9	x		20	0	0	9	255	20			
21	0	0	10	0		21	0	0	10	0	21			
22	0	0	10	x		22	0	0	10	255	22			
23	0	0	11	0		23	0	0	11	0	23			
24	0	0	11	x		24	0	0	11	255	24		<b>_</b>	

Figure 5-7 Rule initialization



#### 5.6 Searching key data

To search key data by the hardware of tCAM-IP demo, the step is following as below and Figure 5-8.

- 1) On SignalTap, setup trigger condition when keyValid = '1' and other signals are don't care. Then press "Run Analysis" button.
- 2) Click "Search" button to run key data searching.
- 3) When search is completed, the message box will popup "Search completed"
  - SignalTap will show all signals interface of tCAM-IP as shown in Figure 5-9
  - In case to see the different trigger point, user can change trigger condition in SignalTap on step 1).
- 4) Result of key search will be displayed to 'Result' column. "rLantencyCount: X" show number of clocks between first key data to first result data.

		Rule	e table		^			Key	data			(	4 le width tCAM-IP version
No.	A+0	A+1	A+2	A+3		No.	A+0	A+1	A+2	A+3	Expect	Result	4 24-bit
1	0	0	0	0		1	0	0	0	0	1	1	☑ 32-bit
2	0	0	0	x		2	0	0	0	255	2	2	
3	0	0	1	0		3	0	0	1	0	3	3	Rule Creation
4	0	0	1	x		4	0	0	1	255	4	4	Pattern 250 60 15 1 From Patter
5	0	0	2	0		5	0	0	2	0	5	5	File 1\software\dataTest\test0001.txt From File
6	0	0	2	x		6	0	0	2	255	6	6	
7	0	0	3	0		7	0	0	3	0	7	7	Key Creation
8	0	0	3	x		8	0	0	3	255	8	8	Number of key : 53796 / 489952
9	0	0	4	0		9	0	0	4	0	9	9	Generate from Rule Stop Shuffle K
10	0	0	4	x		10	0	0	4	255	10	10	
11	0	0	5	0		11	0	0	5	0	11	11	File n\software\dataTest\test0001.txt From Fil
12	0	0	5	x		12	0	0	5	255	12	12	
13	0	0	6	0		13	0	0	6	0	13	13	Hardware Connection
14	0	0	6	x		14	0	0	6	255	14	14	Status code : 1 (initial completed)
15	0	0	7	0		15	0	0	7	0	15	15	
16	0	0	7	x		16	0	0	7	255	16	16	
17	0	0	8	0		17	0	0	8	0	17	17	Search Compare
18	0	0	8	x		18	0	0	8	255	18	18	rLatencyCount : 7
19	0	0	9	0		19	0	0	9	0	19	19	
20	0	0	9	×		20	0	0	9	255	20	20	<b>—</b>
21	0	0	10	0		21	0	0	10	0	21	21	
22	0	0	10	x		22	0	0	10	255	22	22	
23	0	0	11	0		23	0	0	11	0	23	23	
24	0	0	11	x		24	0	0	11	255	24	24	

# Figure 5-8 Search key data

% SignalTap II Logic Ar File Edit View Project				on/intel/tCAMIPT	est - tCAMIPTes	t - [stp1.stp]*								Search alte	
														Ocaren arte	0.0011
Instance Manager: 🍡 🍕	) 🔳 🎦 Read	y to acquire								×	JTAG CH	ain Configu	ration: JTAC	G ready	
nstance 🛃 auto_signaltap_0	Status Not running	Enabled	LEs: 1183 1183 cells	Memory: 16896 16896 bits	Small: 0/185200 0 blocks	Medium: 2/2131 2 blocks	Large: 0/0 0 blocks				Device:			I] • ES 3 3E2 3 •	Setur Scan C
log: Trig @ 2020/05/26 1	4:23:43 (0:0:4.7 elap						click 1	to insert time I	bar		1				
tCAMIP:u_tCA	tCAMIP keyData[31. MIP resultValid	· _	-1 0006310Ah	0 1 X00000000hXFF	2 000000hX0001000		5 0020000hXFF020	6 1000hX0003000							
P Data Setup	tCAMIP resultData[3	<			0000526	iOn			20000001	,000000	<u>12h,000000</u>	<u>103h700000</u>	<u>004h7000000</u>	005hX00000006	nX000000
Hierarchy Display: ✓ ✓ ● tCAMIPTest ✓ ● tCAMIP:u_tC		Data Log:													
🕄 auto_signaltap_0														03	6 00:0

#### Figure 5-9 Sample of SignalTap result



#### 5.7 Compare

To compare between the expected value (from software) and result from hardware searching, the step is as shown in Figure 5-10.

- 1) Click "Compare" button to compare expect data and result data of key data.
- 2) When comparing is completed, if compare have mismatch. The message box will popup "Completed with X mismatch found", By X is number of mismatches found.

		Rule	e table		^			Key	data			^	Rule width tCAM-IP version : 1.
No.	A+0	A+1	A+2	A+3		No.	A+0	A+1	A+2	A+3	Expect	Result	24-bit
1	0	0	0	0		1	0	0	0	0	1	1	☑ 32-bit
2	0	0	0	x		2	0	0	0	255	2	2	
3	0	0	1	0		3	0	0	1	0	3	3	Rule Creation
4	0	0	1	x		4	0	0	1	255	4	4	Pattern 250 60 15 1 From Pattern
5	0	0	2	0		5	0	0	2	0	5	5	File 1\software\dataTest\test0001.txt From File
6	0	0	2	x		6	0	0	2	255	6	6	
7	0	0	3	0		7	0	0	3	0	7	7	Key Creation
В	0	0	3	x		8	0	0	3	255	8	8	Number of key : 53796 / 489952
9	0	0	4	0		9	0	0	4	0	9	9	Generate from Rule Stop Shuffle Key
10	0	0	4	x		10	0	0	4	255	10	10	
11	0	0	5	0		11	0	0	5	0	11	11	File n\software\dataTest\test0001.txt From File
12	0	0	5	x		12	0	0	5	255	12	12	
13	0	0	6	0		13	0	0	6	0	13	13	Hardware Connection
14	0	0	6	x		14	0	0	6	255	14	14	Status code : 1 (initial completed)
15	0	0	7	0		15	0	0	7	0	15	15	
16	0	0	7	x		16	0	0	7	255	16	16	Disconnect Rule init 1
17	0	0	8	0		17	0	0	8	0	17	17	Search Compare
18	0	0	8	x		18	0	0	8	255	18	18	rLatencyCount : 7
19	0	0	9	0		19	0	0	9	0	19	19	
20	0	0	9	x		20	0	0	9	255	20	20	
21	0	0	10	0		21	0	0	10	0	21	21	
22	0	0	10	x		22	0	0	10	255	22	22	
23	0	0	11	0		23	0	0	11	0	23	23	
24	0	0	11	x		24	0	0	11	255	24	24 🗸	

Figure 5-10 Step to compare data.



# 6 Revision History

Revision	Date	Description							
1.0	1-Jul-2020	Initial version release							