tCAM-IP Demo Instruction

Rev1.0 1-Jul-20

This document describes the instruction to demonstrate the operation of tCAM-IP on Arria10SoC development boar. This demonstration uses tCAM-IP demo software to communicate with development board via 1-Gb Ethernet for preparing rule table, initializing tCAMP-IP, sending keys and reading result data. User is also able to use SignalTap to see the operation of provided signal in FPGA.

1 Environment Setup

To operate tCAM-IP demo, please prepare following test environment.

1) FPGA development boards (Arria10SoC development board)
2) Test PC with 1-Gb Ethernet connection.
3) Micro USB cable for JTAG connection connecting between FPGA development board and PC
4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA development board and PC
5) Quartus Prime for programming FPGA, installed on Test PC
6) File “tCAMIPDemoPack.zip” that included Test Application named “tCAM-IP Demo”, configuration file named “tCAMIPTest_time_limited.sof” and SignalTap file named “stp1.stp”.
   (to download this file, please visit our web site at www.design-gateway.com)

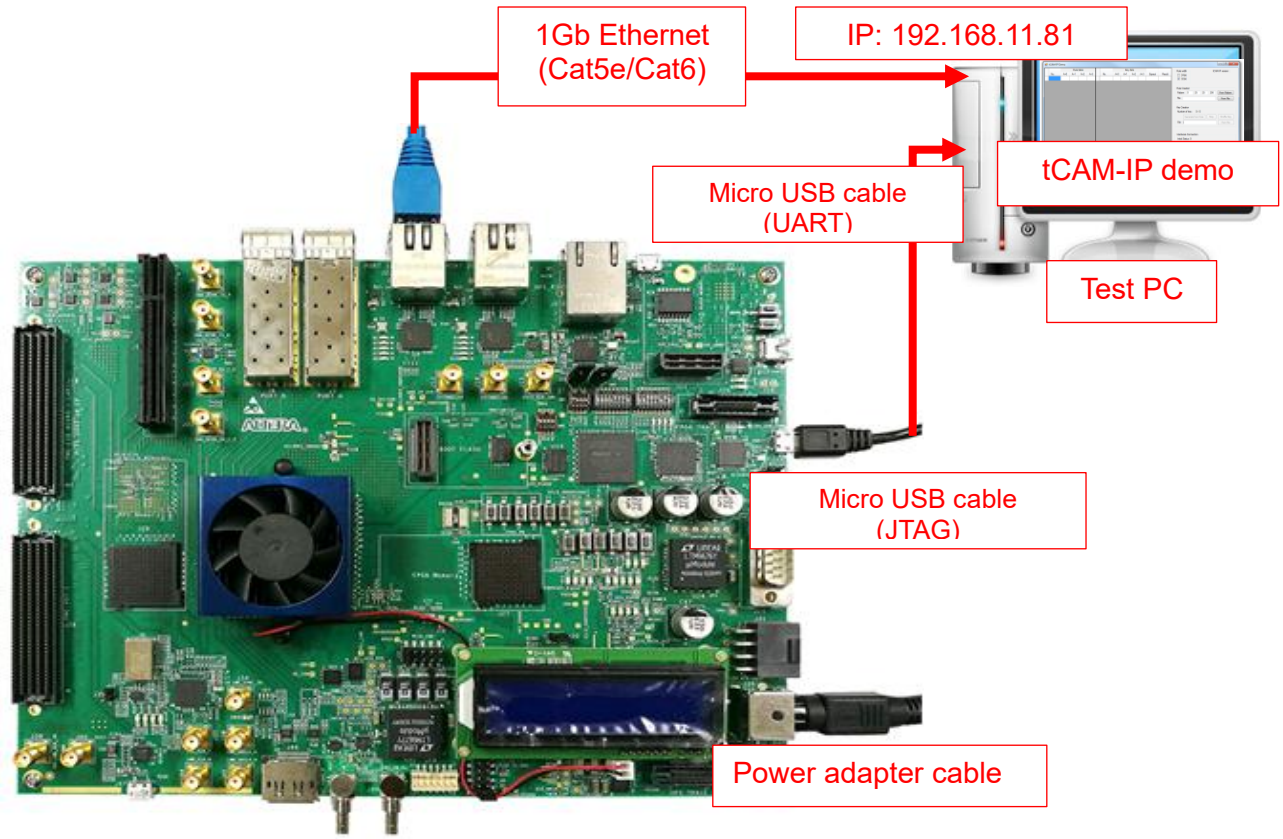

Figure 1-1 tCAM-IP demo (FPGA<->PC) on Arria10SoC board

2 PC Setup

Before running demo, please check the network setting on PC. Ethernet setting is shown as follows.

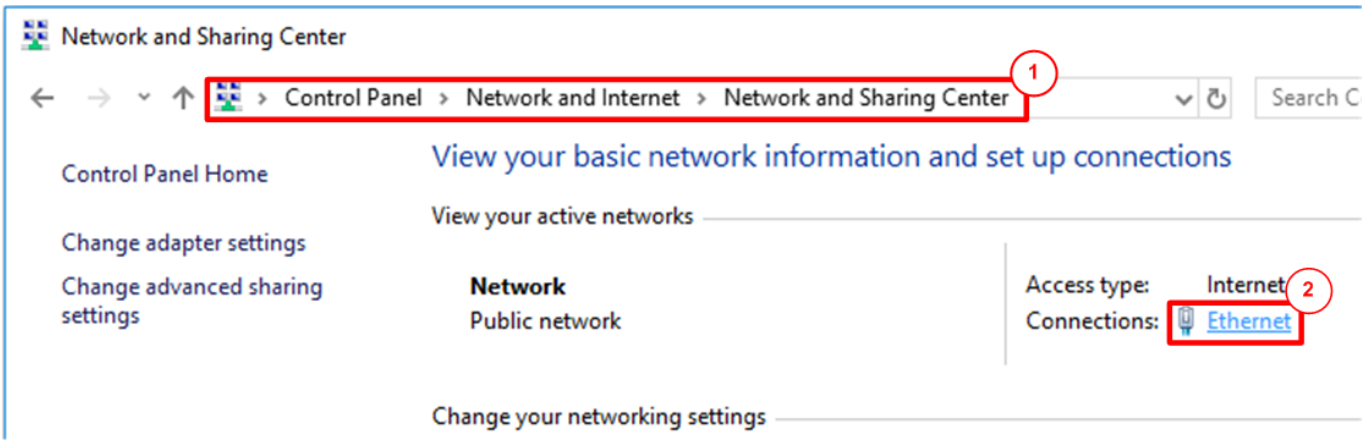

Figure 2-1 IPv4 setting

1) Open Ethernet setting option from Control Panel -> Network and Internet -> Network and Sharing Center.
2) Click Ethernet icon which is used to connect with FPGA board.

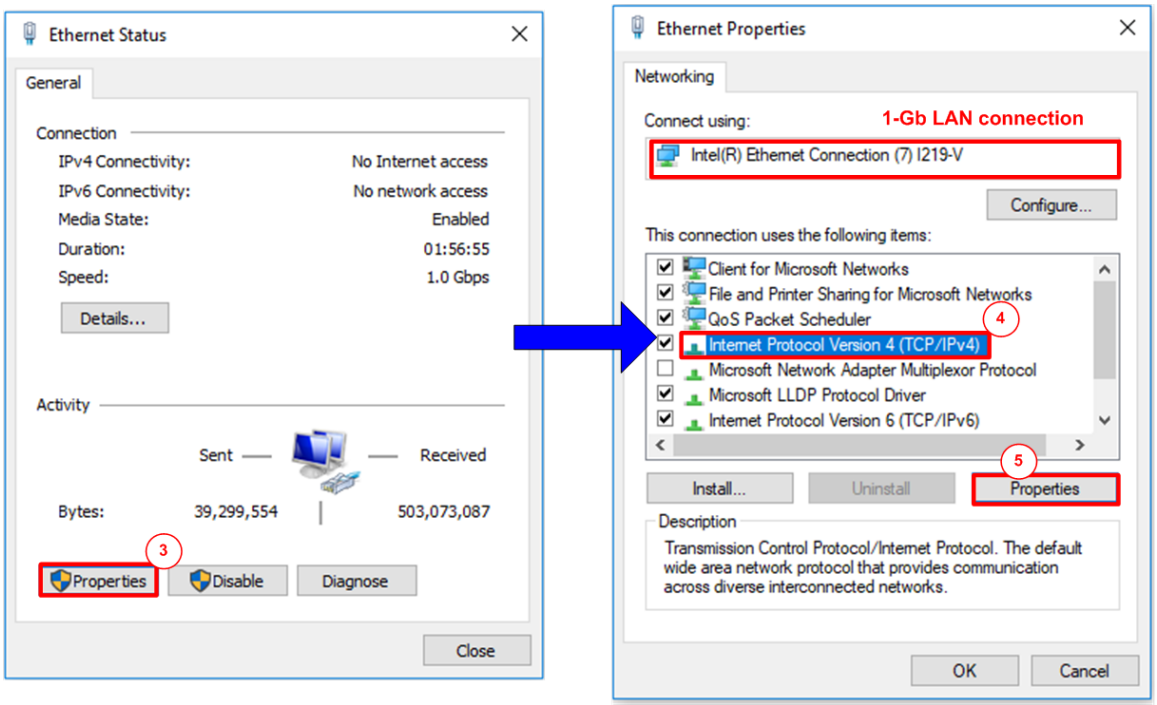

Figure 2-2 Select IP address setting menu

3) Click Properties button in Ethernet Status window.
4) Select “TCP/IPv4”.
5) Click Properties button in Ethernet Properties window.

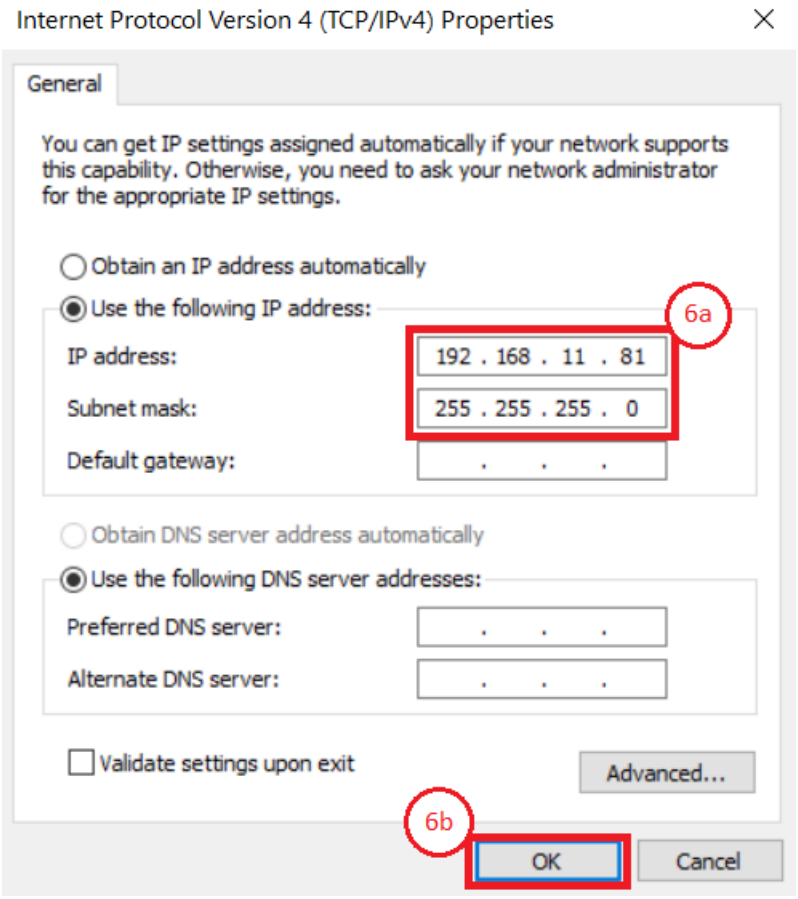

Figure 2-3 Set IP address

6) Set IP address = 192.168.11.81 and Subnet mask = 255.255.255.0. After that, click OK button to confirm IP address setting.

3 FPGA board setup

1) Make sure power switch is off and connect power supply to FPGA development board.
2) Connect USB cable between FPGA board and PC via micro USB
3) Connect CAT5e/CAT6 cable between PC and Ethernet connection of FPGA board. User must use the right port when FPGA board has two 1Gb Ethernet ports.

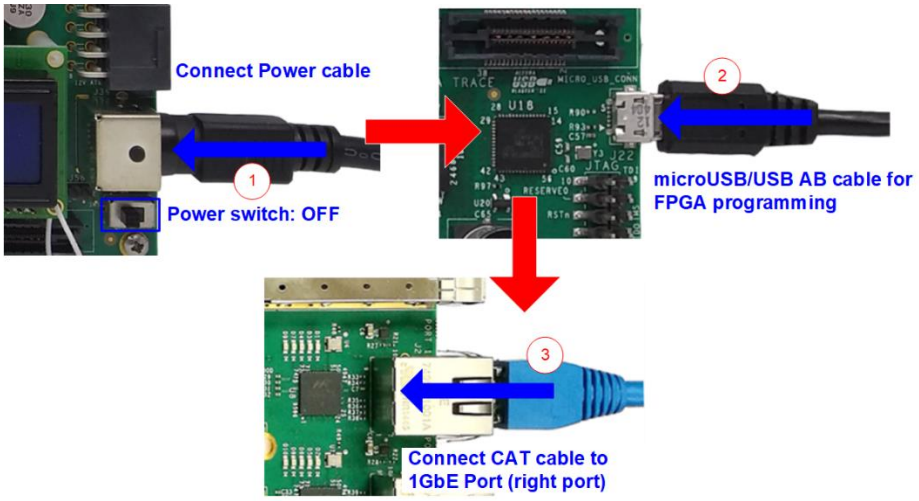

Figure 3-1 Power, Ethernet, and micro USB cable connection

4) Power on system.
5) Open QuartusII Programmer to program FPGA through USB-1 by following step.
   a) Click “Hardware Setup…” to select USB-BlasterII [USB-1].
   b) Click “Auto Detect” and select FPGA device. (10AS066N3).
   c) Select FPGA device icon.
   d) Click “Change File” button, select SOF file in pop-up window, and click “open” button
   e) Check “program”
   f) Click “Start” button to program FPGA and wait until Progress status is equal to 100%

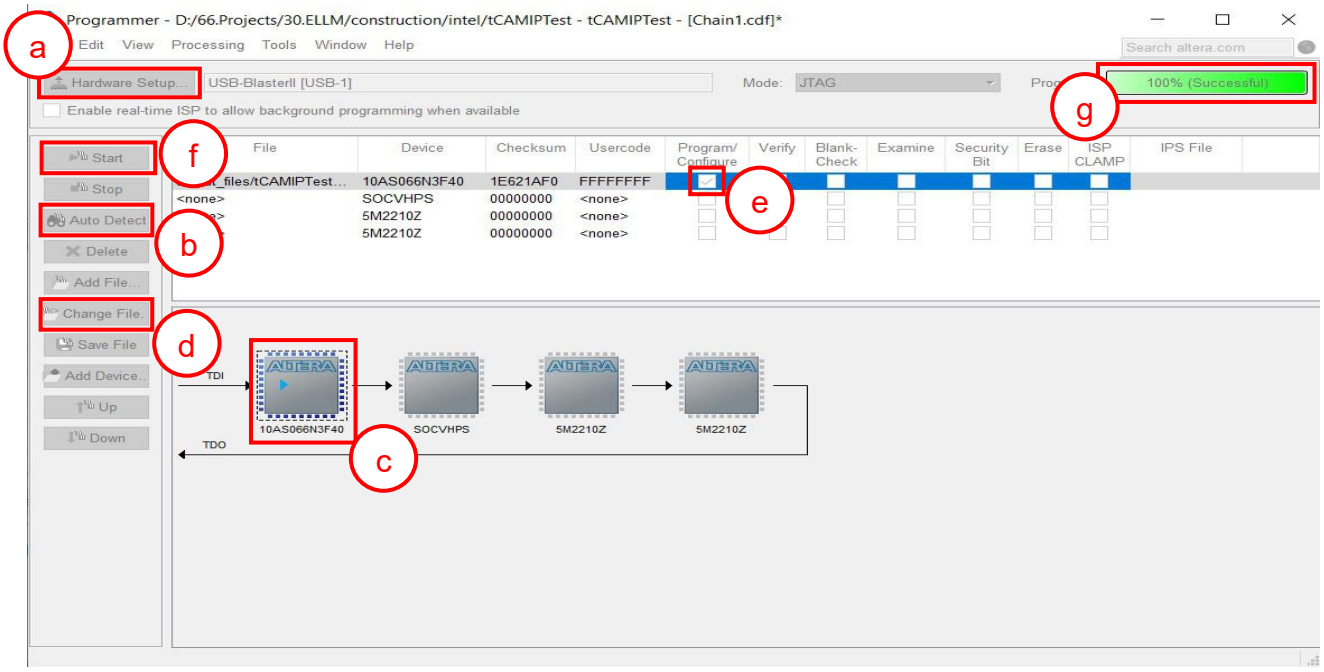

Figure 3-2 FPGA Programmer

6) When configuration is completed, user can check status LEDs on board as Figure 3-3
   - LED#1 is always blink to show clock is working.
   - LED#2 is tcamRstB signal. This LED#2 is related to hardware reset switch “S10”.
   - LED#3 is “Connection on” status of TOE1G-IP. This LED is on when software open connection to board.
   - LED#4 is “Ready” status of TOE1G-IP. This LED is on when ethernet connection between PC and board is ready.

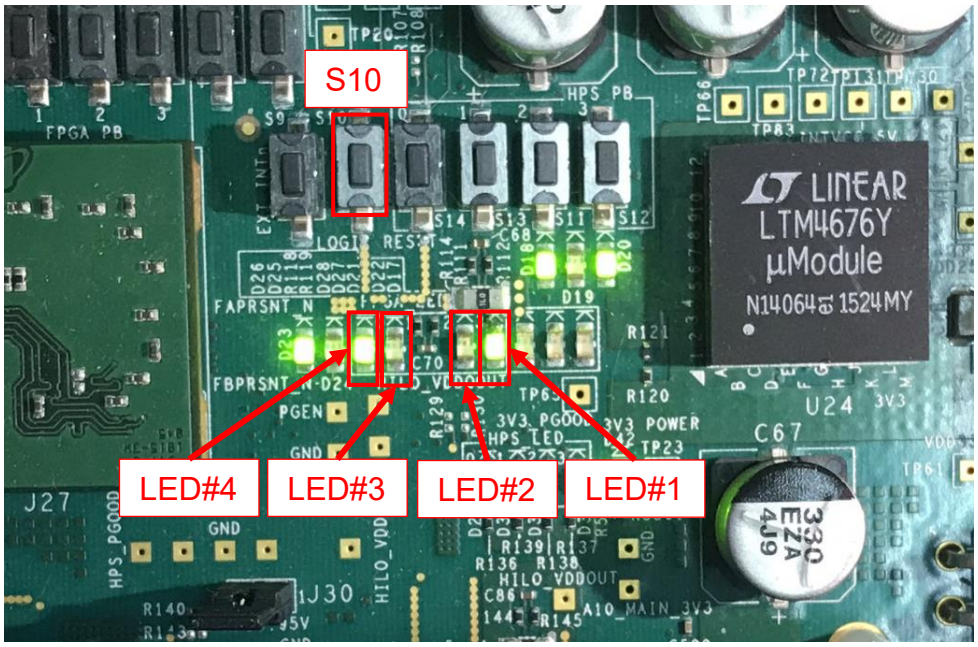

Figure 3-3 LEDs status on board

4 SignalTap setup

This designed block diagram of this demo is shown as in Figure 4-1. SignalTap is prepared to see all control signals between tCAM-IP and user logics design.

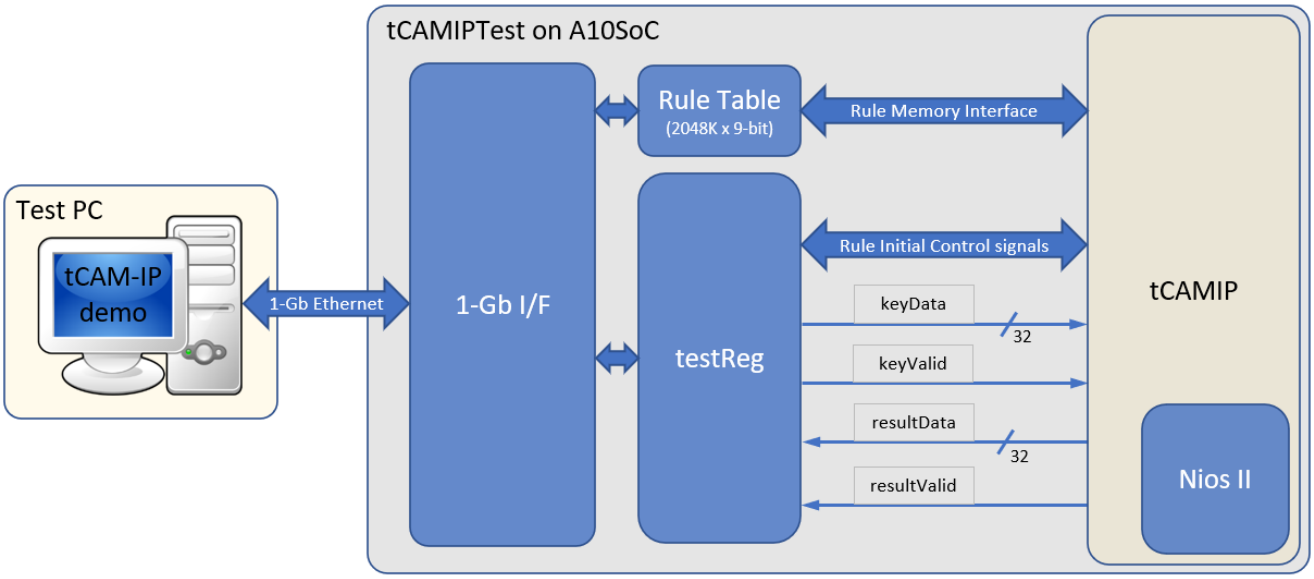

Figure 4-1 Demo environment block diagram

4.1 SignalTap operations

Step to use SignalTap II Logic Analyzer is as follows.

a) Click File -> Open …, then select file type to SignalTap II Logic Analyzer Files (*.stp)
b) Select “stp1.stp”, then click Open button as shown in Figure 4-2
c) As in Figure 4-3, connect FPGA board by select Hardware to USB-BlasterII.
d) Setup trigger condition to specify signals behavior. Sample of trigger condition and result is shown as in topic 4.2
e) Click “Run Analysis” button, wait to capture signals from tCAM-IP.
f) The result will be shown, when do SignalTap detect signals same as trigger condition.

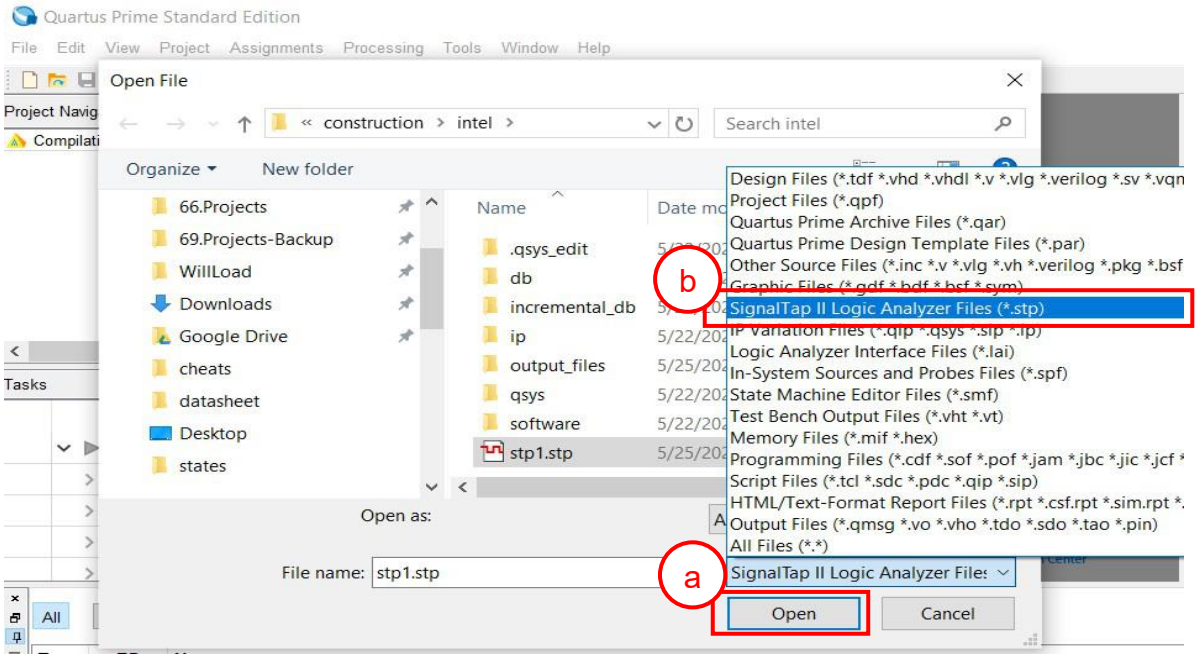

Figure 4-2 Open file “stp1.stp”

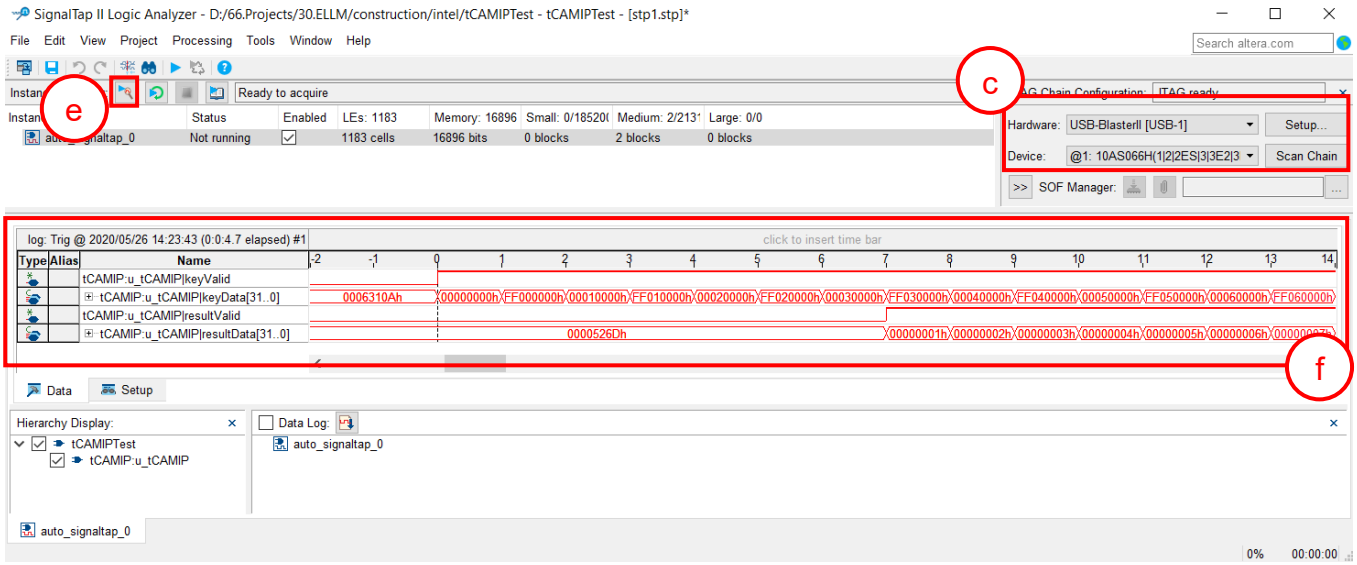

Figure 4-3 SignalTap II Logic Analyzer

4.2 SignalTap trigger condition

On demo running, user is able to use SignalTap to setup trigger condition and check the signal waveform after trigger is detected. The prepared SignalTap signals are separated to 3 parts as (1) Rule Initial control signals, (2) Rule Memory interface signals and (3) Input keys & search result signal respectively.

4.2.1 To see Rule Initial Control signals

Figure 4-4 show trigger condition and Figure 4-5 show sample result from SignalTap when user do initial rule table in topic 0

trigger: 2020/05/27 16:23:21 #0 — Lock mode: Allow all changes

Node			Data Enable	Trigger Enable	Trigger Conditions
Type	Alias	Name	186	186	1 Basic AND
		tCAMIP:u_tCAMIP|ruleWidth[15..0]	☑	☑	XXXXh
		tCAMIP:u_tCAMIP|ruleCount[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|ruleInit	☑	☑	1
		tCAMIP:u_tCAMIP|ruleBusy	☑	☑	
		tCAMIP:u_tCAMIP|ruleAddr[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|ruleRdReq	☑	☑	
		tCAMIP:u_tCAMIP|ruleRdValid	☑	☑	
		tCAMIP:u_tCAMIP|ruleData[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|ruleStatusCode[3..0]	☑	☑	Xh
		tCAMIP:u_tCAMIP|keyValid	☑	☑	
		tCAMIP:u_tCAMIP|keyData[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|resultValid	☑	☑	
		tCAMIP:u_tCAMIP|resultData[31..0]	☑	☑	XXXXXXXXh

Figure 4-4 Trigger setup for rule initial control signals

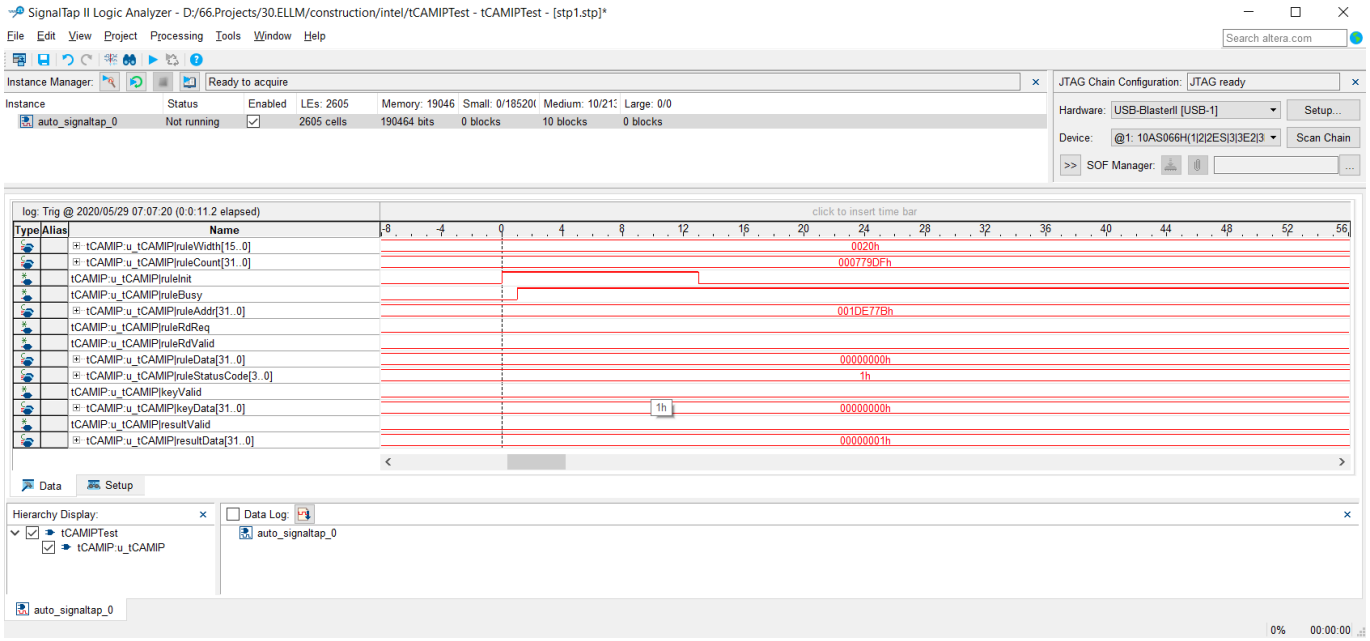

Figure 4-5 Sample result for rule initial control signals

4.2.2 To see Rule Memory Interface signals

Figure 4-6 show trigger condition and Figure 4-7 show sample result from SignalTap when user do initial rule table in topic 0

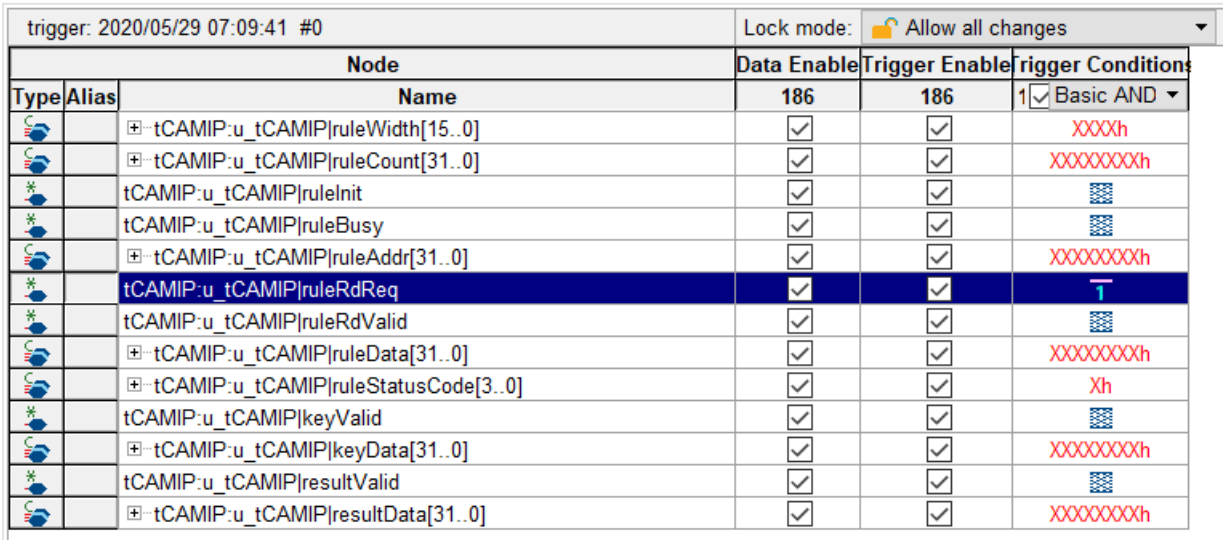

Figure 4-6 Trigger setup for rule memory signals

Figure 4-7 Sample result for rule memory signals

4.2.3 To see Input key and Search result signals

Figure 4-8 show trigger condition and Figure 4-9 show sample result from SignalTap when user do initial rule table in topic 5.6

trigger: 2020/05/29 07:09:41 #0 — Lock mode: Allow all changes

Node			Data Enable	Trigger Enable	Trigger Conditions
Type	Alias	Name	186	186	1 Basic AND
		tCAMIP:u_tCAMIP|ruleWidth[15..0]	☑	☑	XXXXh
		tCAMIP:u_tCAMIP|ruleCount[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|ruleInit	☑	☑	
		tCAMIP:u_tCAMIP|ruleBusy	☑	☑	
		tCAMIP:u_tCAMIP|ruleAddr[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|ruleRdReq	☑	☑	
		tCAMIP:u_tCAMIP|ruleRdValid	☑	☑	
		tCAMIP:u_tCAMIP|ruleData[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|ruleStatusCode[3..0]	☑	☑	Xh
		tCAMIP:u_tCAMIP|keyValid	☑	☑	1
		tCAMIP:u_tCAMIP|keyData[31..0]	☑	☑	XXXXXXXXh
		tCAMIP:u_tCAMIP|resultValid	☑	☑	
		tCAMIP:u_tCAMIP|resultData[31..0]	☑	☑	XXXXXXXXh

Figure 4-8 Trigger setup for input key and searching result

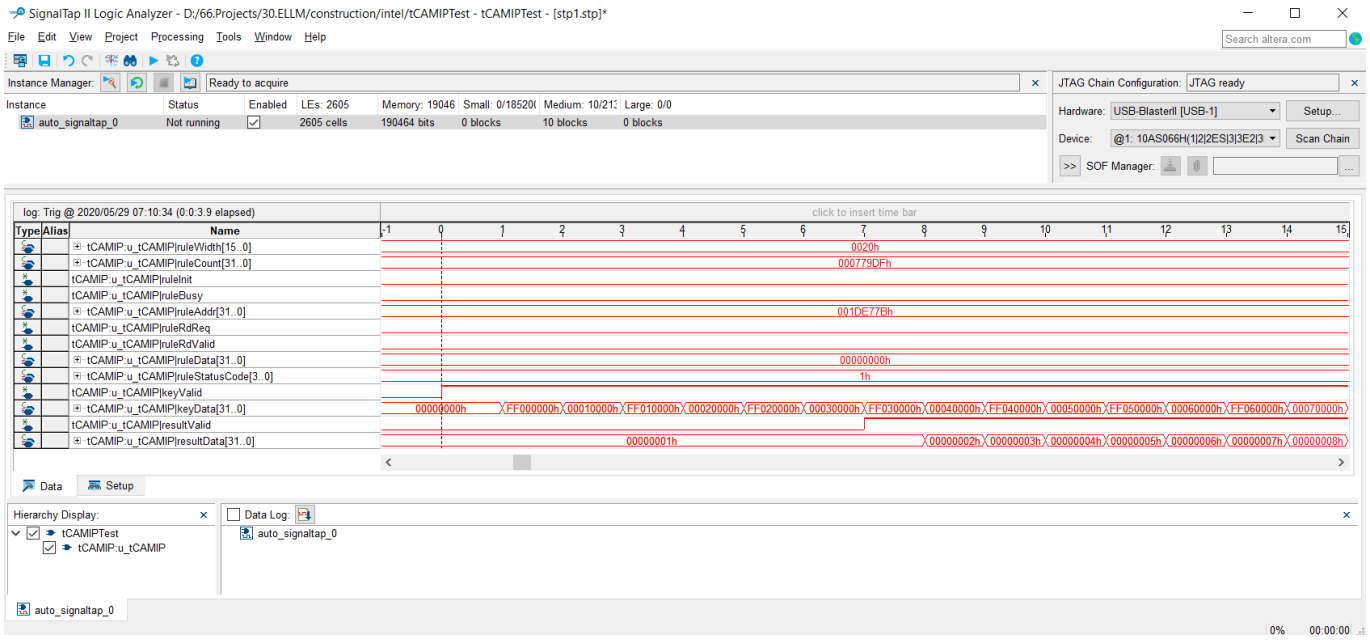

Figure 4-9 Sample result for input key and searching result

5 tCAM-IP demo software

tCAM-IP demo software is used for preparing and sending rule and key pattern data to A10SoC board via 1-Gb Ethernet connection and getting the result of searching from tCAM-IP.

The main features of tCAM-IP demo software are as following.

1) Rule creation.
2) Key creation.
3) Initialization rule data table to FPGA development board.
4) Search key data and display result.
5) Compare expect data of key data searching to result data of key data searching.

5.1 Demo software interface description

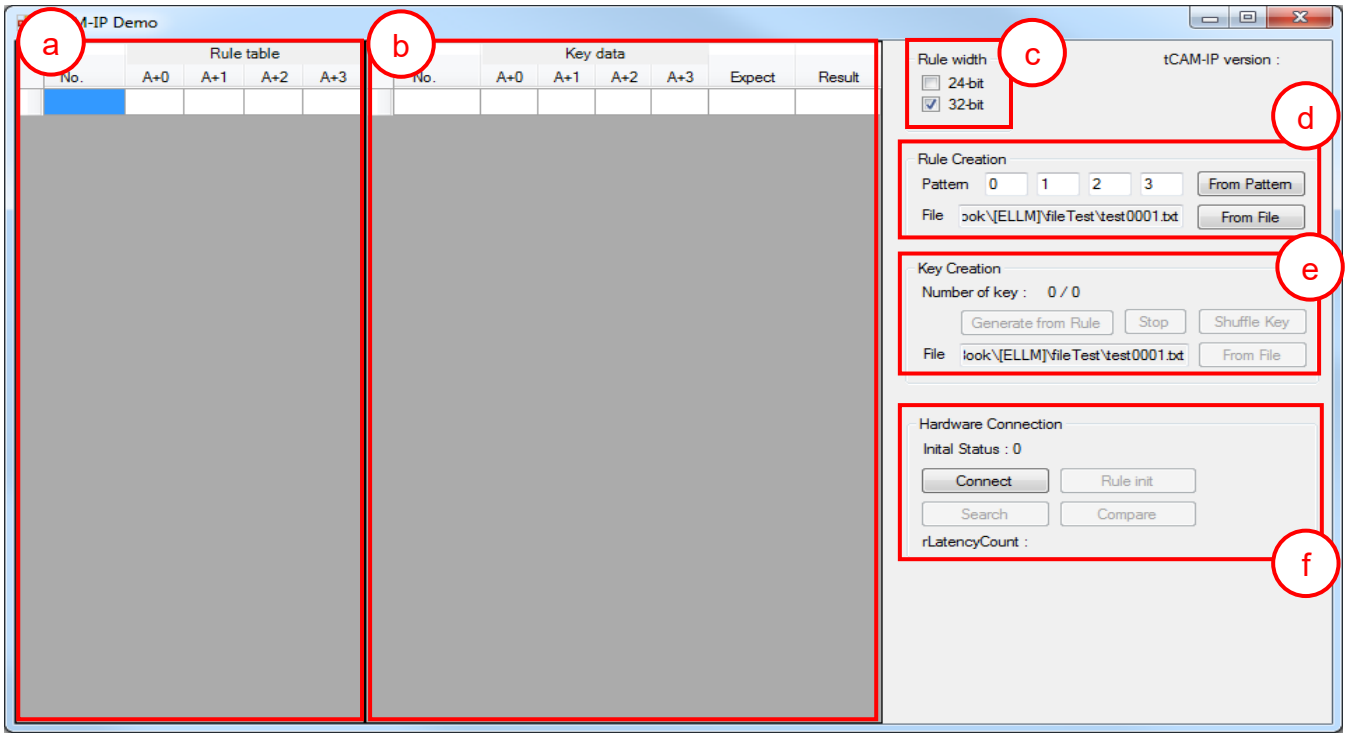

Figure 5-1 Software interface

Figure 5-1 shows tCAM-IP demo software and the description is shown as below.

a) Rule table is the user rule data display.
b) Key data table is the user key data display.
c) Rule width, Users can select data size modes.
d) Rule Creation, Users can generate rule data table pattern or load rule data table pattern from the file.
e) Key Creation, Users can generate key data from rule table or load key data table pattern from the file.
f) Hardware Connection, Users can communicate with FPGA development board in this part. Which consists of connection with board, rule Initialize, key data search, result compare.

5.2 File format for Rule data and Key Data

User can prepare Rule data or Key data file for this demo. The file format is shown as Figure 5-2**Error! Reference source not found.** and Figure 5-3 for rule width 32-bit and 24-bit respectively.

1) The first line is header of file for specific number of byte data in this file like “A+0, A+1, A+2, A+3” for 32-bit file format.
2) Next lines are data. The valid range of data is 0-255, others number and ‘x’ is defined to don’t care value.

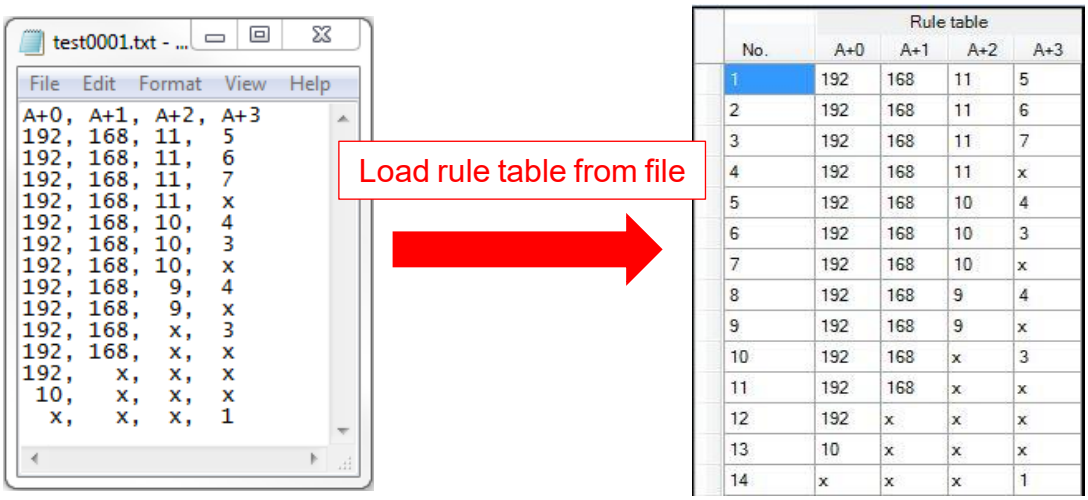

Figure 5-2 Example of load rule file 32-bit

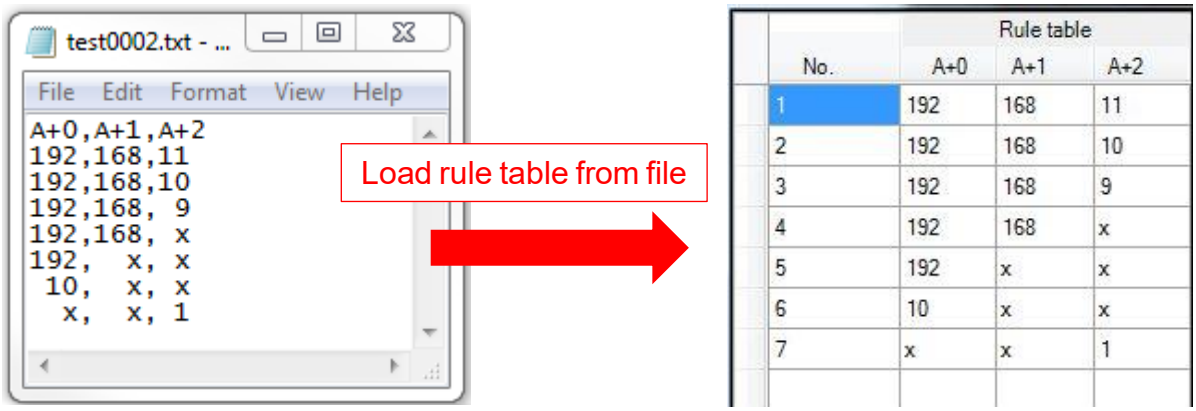

Figure 5-3 Example of load rule file 24-bit

5.3 Rule table creation

To create the rule table, the step is shown as in Figure 5-4.

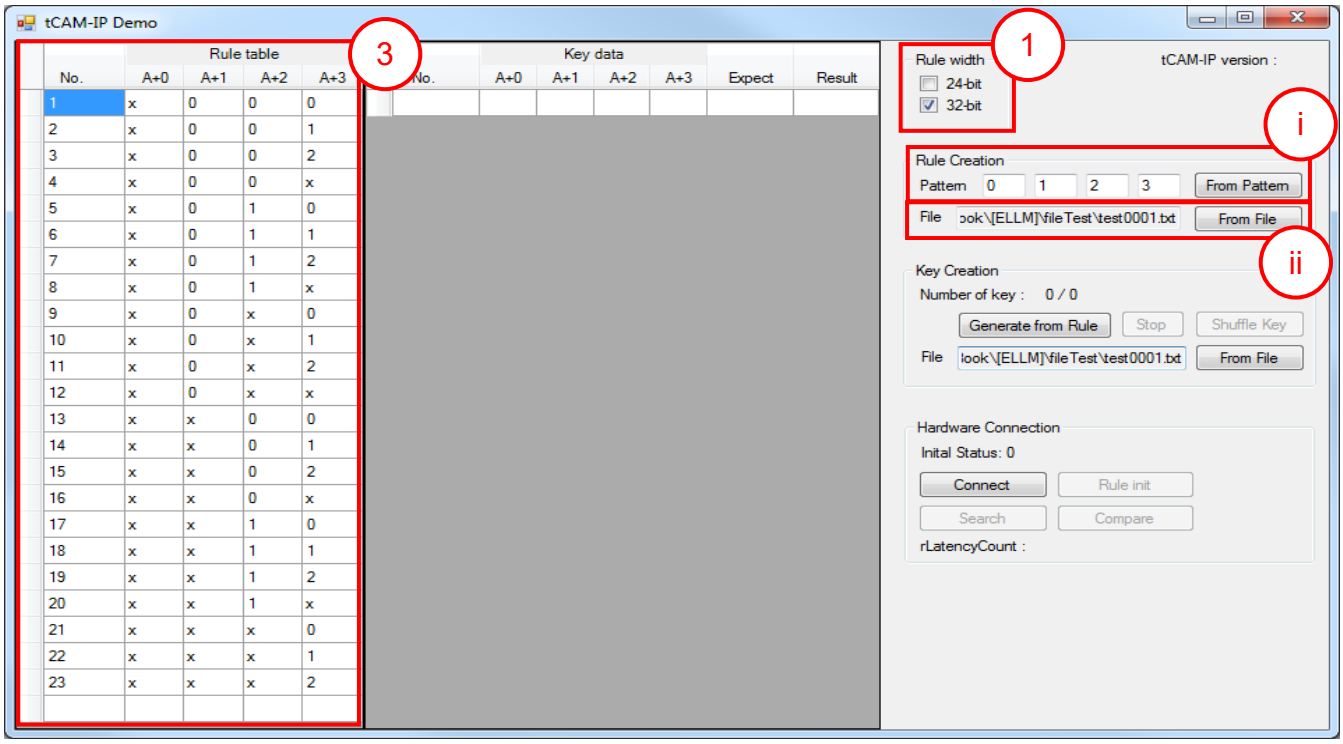

Figure 5-4 Rule creation process

1) Select Rule width mode for setup data size.
2) Create rule table, the user can select 2 modes as follows.
   i) Generate rule data table from pattern as show in Figure 5-5.
      a) Fill out valid range (0-256) of each byte in “Pattern”. Byte of pattern position starts “A+0” left to right.
      b) Click “From Pattern” to start generate rule table.

Figure 5-5 Example rule data table pattern.

   ii) Load rule data table from the file by click “From File” button to browse and load rule data file.
3) When rule is created, rule data show in rule table as shown in Figure 5-4.

5.4 Key data table creation

To create key table, the step is shown as in Figure 5-6.

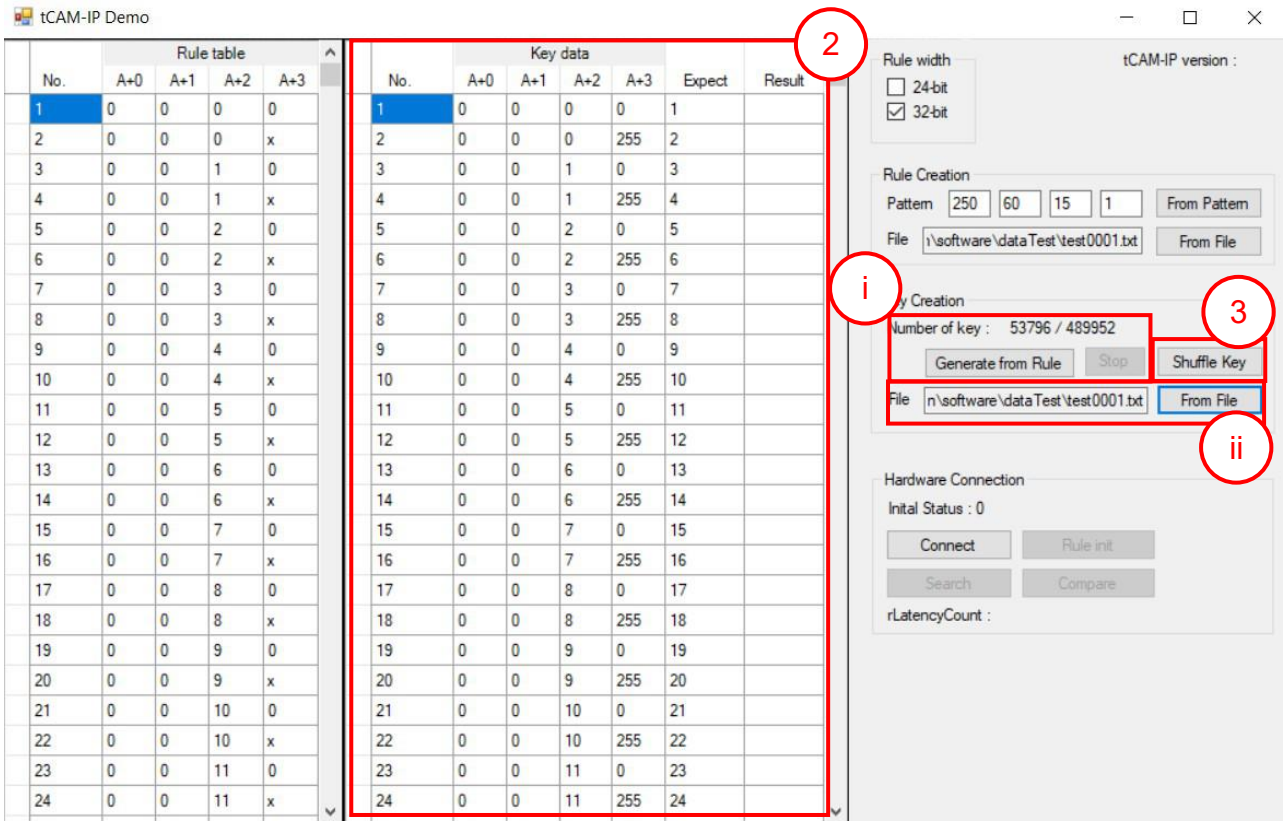

Figure 5-6 Key creation

1) Create Key data, the user can select 2 modes as follows
   i) Generate key data from rule table.
      a) Click “Generate from Rule” to start generate key data.
      b) “Number of key: X / Y” is progress status by X is progress number of key and Y is total number of keys from all combination of rules. (generating time depends on the amount of key data)
      c) “Stop” button is used for stop key generating.
   ii) Load key data from the file by click “From File” button to browse and load rule data file.
2) When key data is created, the expect value will be generated automatically.
3) “Shuffle Key” button is used to shuffle each key in key table randomly.

5.5 Initialization rule data to FPGA Development board

The step to initialize rule data is following as below and Figure 5-7.

1) Please make sure that LED#4 is on (ready), before click “Connect” button.
2) When connection is completed, the text of the button will change to “Disconnect” and LED#3 is turn on (please refer LEDs on board in Figure 3-3). The button “Rule init”, “Search” and “Compare” will enable.
3) On SignalTap, setup trigger condition when ruleInit = ’1’ and other signals are don’t care. Then press “Run Analysis” button.
4) Click “Rule init” button to initialize data of rule table. Initializationi duration time depends on the amount of key data.

   “Initial Status: X” is active status for Rule transfer, Rule verify, Rule initial and Status code. By X is running umber of rule table, time count of Rule initial status and status code which shows that process is still running)
   - When ruleInit signal = ‘1’, SignalTap will show all interface signals of tCAM-IP.
   - In case to see the difference trigger point, user can change trigger condition in SignalTap on step 3).
5) When initialization is completed, the message box will popup “Rule initial completed”. In case initialization is incompleted, “Initial Status:” is shown error message of status code.

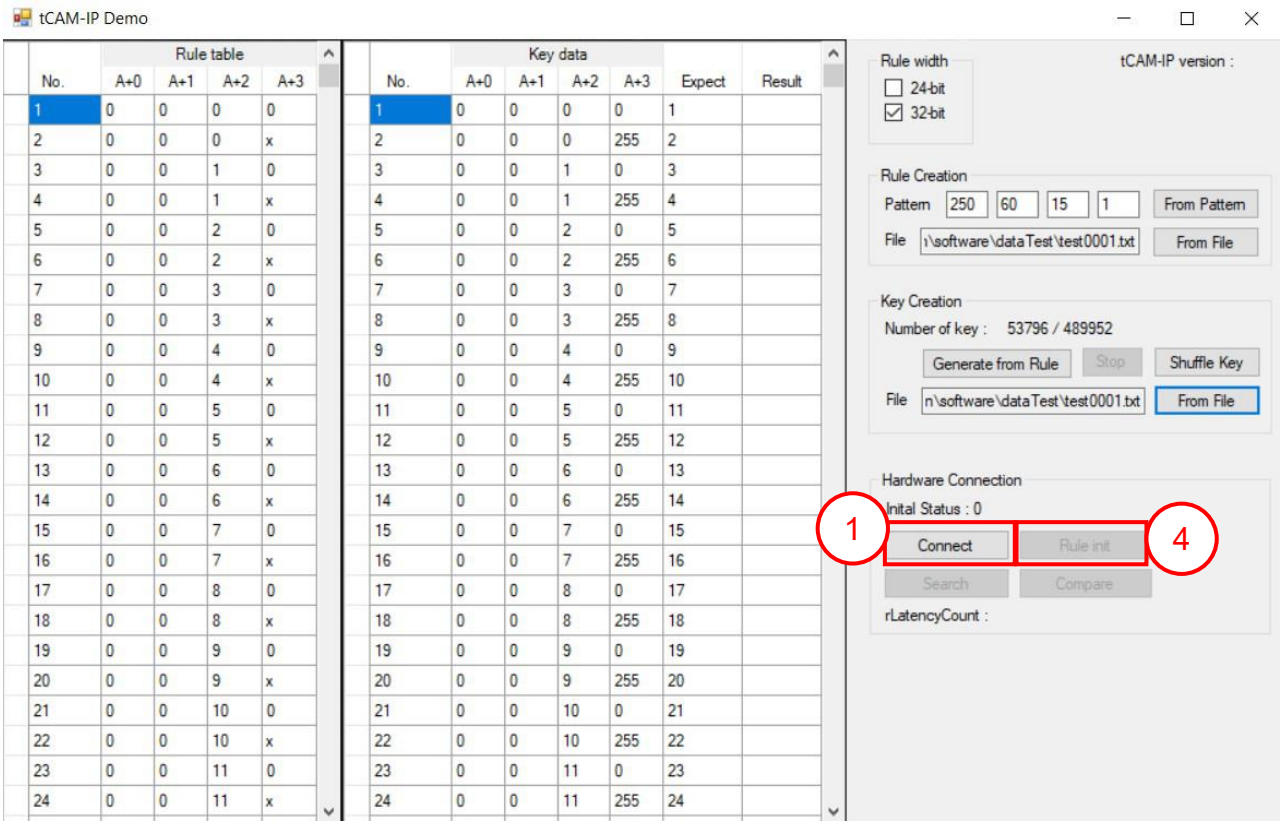

Figure 5-7 Rule initialization

5.6 Searching key data

To search key data by the hardware of tCAM-IP demo, the step is following as below and Figure 5-8.

1) On SignalTap, setup trigger condition when keyValid = '1' and other signals are don't care. Then press "Run Analysis" button.
2) Click "Search" button to run key data searching.
3) When search is completed, the message box will popup "Search completed"
   - SignalTap will show all signals interface of tCAM-IP as shown in Figure 5-9
   - In case to see the different trigger point, user can change trigger condition in SignalTap on step 1).
4) Result of key search will be displayed to 'Result' column. "rLantencyCount: X" show number of clocks between first key data to first result data.

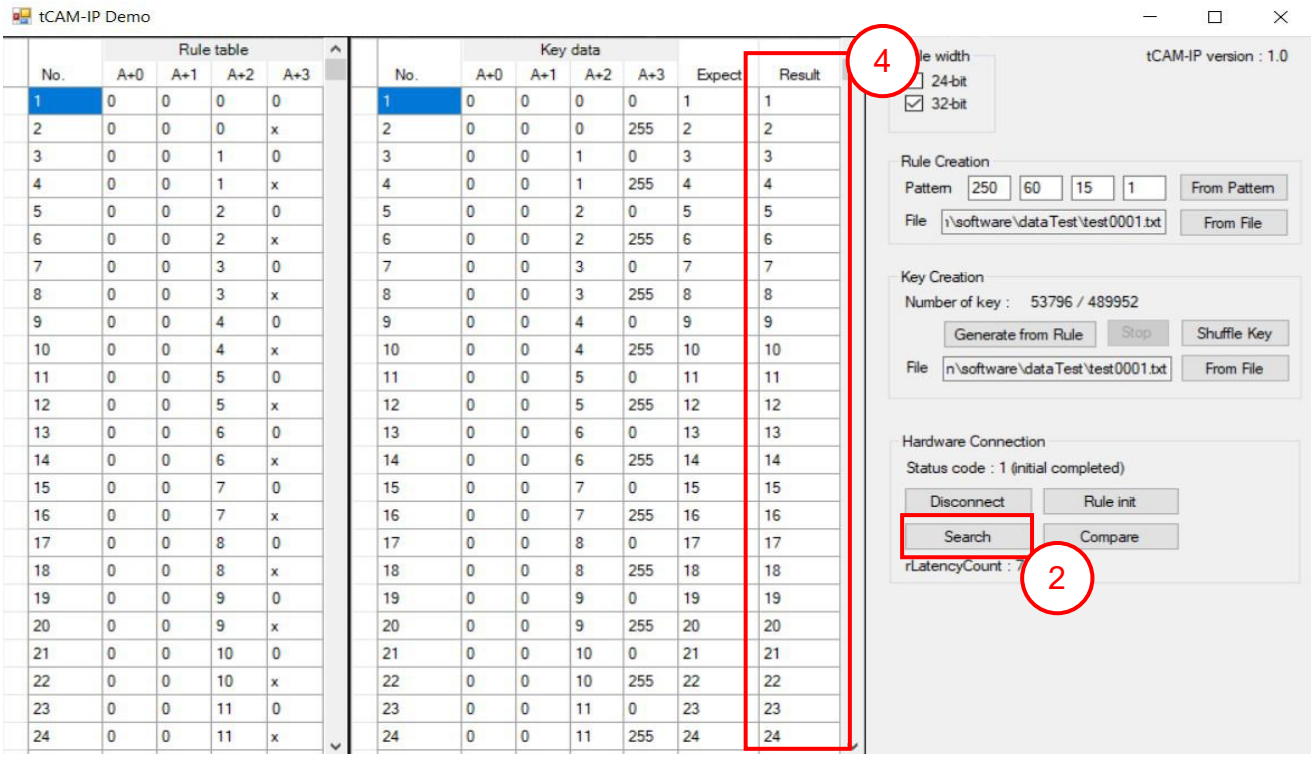

Figure 5-8 Search key data

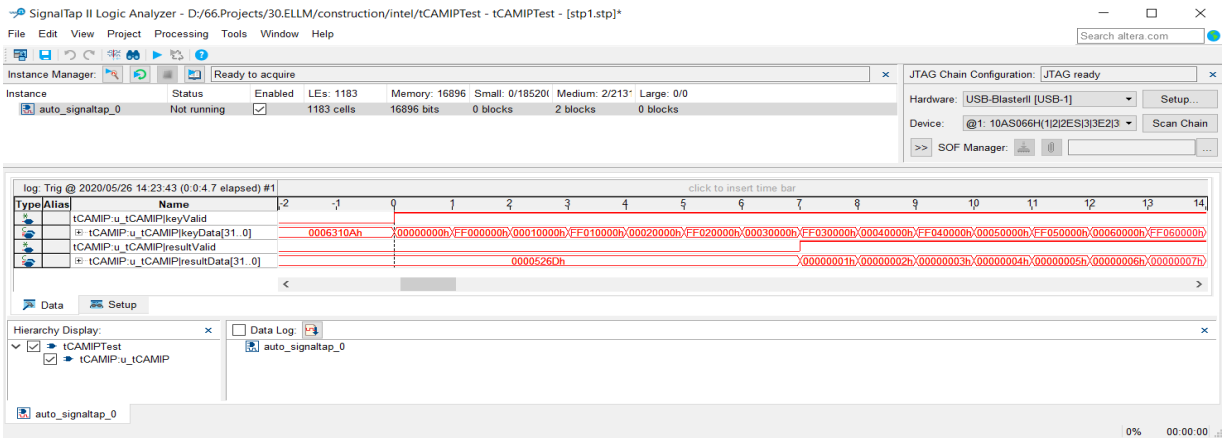

Figure 5-9 Sample of SignalTap result

5.7 Compare

To compare between the expected value (from software) and result from hardware searching, the step is as shown in Figure 5-10.

1) Click “Compare” button to compare expect data and result data of key data.
2) When comparing is completed, if compare have mismatch. The message box will popup “Completed with X mismatch found”, By X is number of mismatches found.

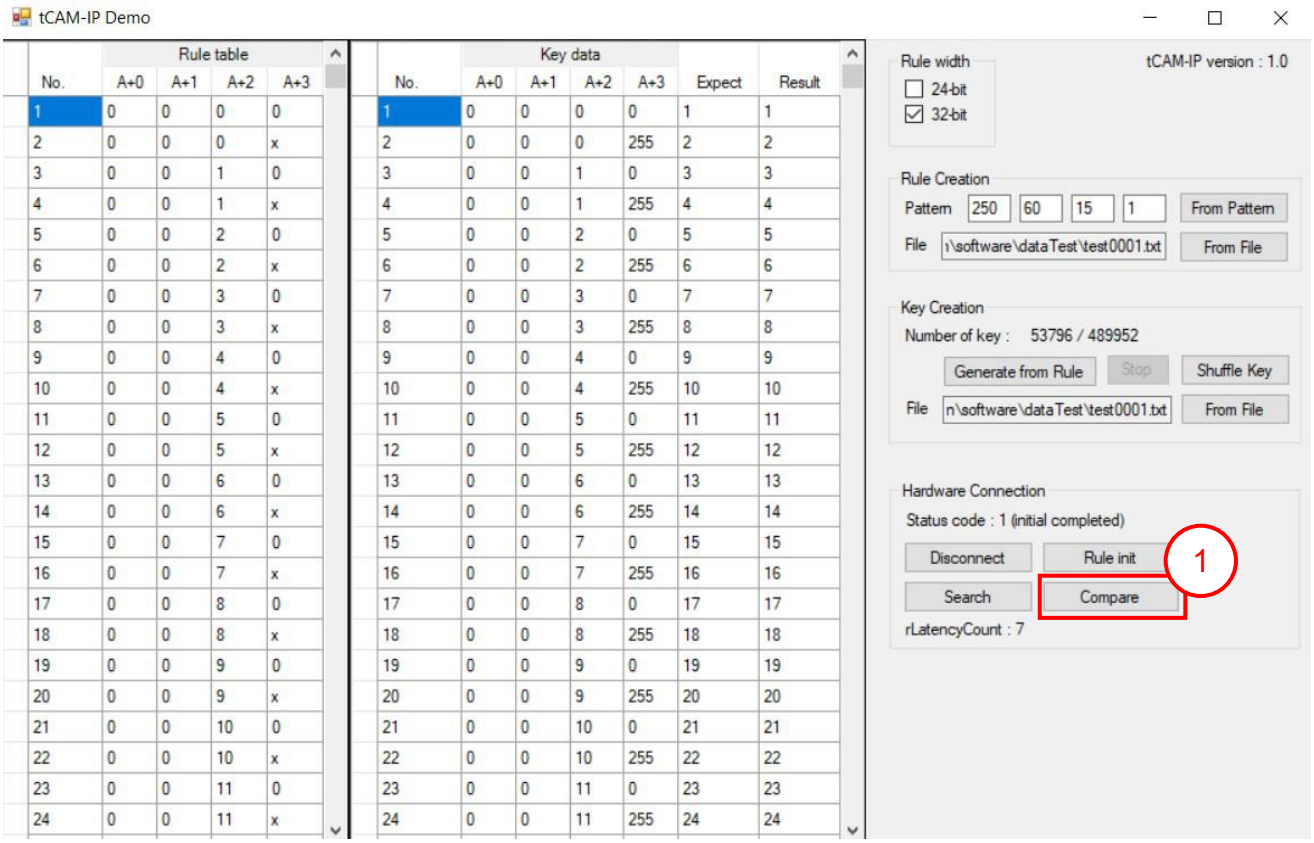

Figure 5-10 Step to compare data.

6 Revision History

Revision	Date	Description
1.0	1-Jul-2020	Initial version release