IP Lock (standard pack)

User's Manual

Design Gateway Co.,Ltd.

Rev 1.7

(PD0602-6-01-07E)

*** Please read this manual carefully before using IP Lock (standard pack)***

Revision History

Revision	Date	Detail of change
1.0	10-May-06	Initial Release
1.1	18-Jul-06	Adding IP lock core for Altera FPGA.
1.2	19-Oct-06	Update detail of setting internal pull-up on ISE Update detail of SC0 signal
1.3	08-Nov-07	Support Xilinx Virtex5 Adding Troubleshooting
1.4	06-Aug-10	Update Figure 4-1 and 4-8
1.5	15-Oct-10	Update Device support
1.6	17-Aug-11	Add resource information
1.7	28-May-19	Update Device support

Table of Contents

1. Product Overview

1.1. Delivery items

Thank you very much for purchasing IP Lock. The product box includes the following items.

1. IP Lock device : 10 pieces or 50 pieces
2. CD ROM : 1 piece
   - IP Lock core (TopIPLock.vhd, iplock.vhd)
   - Example VHDL design source code (Counter.vhd, Counter32Bits.vhd)
   - IP Lock user's manual (IPLSTD_UserManualx_x_E.pdf)

Note: License file is necessary to implement IP Lock core into the user's project file by using FPGA tools (Vivado, ISE, or Quartus). The details to send the request for IP Lock license file are described in topic "2.2 The license file".

1.2. IP Lock core specification

1. 128-bit AES encryption
2. Resource

   Xilinx FPGA (Spartan-7 device) : 318 Slices and 1 BRAM Tiles (36 Kb)

   Intel FPGA (Cyclone10 LP device) : 1,221 LEs and 24,576 Memory bits

   ** Actual logic resource depends on the percentage of unrelated logic
3. Sampling period to check connection status between IP Lock device and IP Lock core:

   Every 200 msec
4. Supported device list

   Please download from https://dgway.com/products/IPLock/IPL-LIST.pdf.

1.3. System Requirement for IP Lock core

1. Xilinx FPGA tool

   a) ISE Design Suite for Spartan6, Virtex6 and the previous generation families

   Please see more details about the system requirement for ISE tool from following link.

   https://www.xilinx.com/products/design-tools/ise-design-suite.html

   https://www.xilinx.com/products/design-tools/ise-design-suite/memory.html

   b) Vivado Design Suite for Virtex7, Kintex7, Artix7, Zynq7000 and the newer families.

   Please see more details about the system requirement for Vivado tool from following link.

   https://www.xilinx.com/products/design-tools/vivado.html

   https://www.xilinx.com/products/design-tools/vivado/memory.html

2. Intel FPGA tool: Quartus tool

   Please check more details about the tools and the system requirement from following link.

   https://www.intel.com/content/www/us/en/programmable/support/support-resources/download/os-support.html

1.4. IP Lock caution

Please confirm the below information when using the IP Lock system.

1. IP Lock core and IP Lock device must be used from the same product box. In the standard pack, IP Lock core and IP Lock device have the unique user's ID. So, the stuffs from different product box cannot communicate successfully.
2. Please check IP Lock device direction before mounting on the Writer and the PCB.
3. Support voltage range of IP Lock device: +1.8V, +2.5V or +3.3V.

1.5. Warranty Policy

1. Product warranty is valid for 1 year from purchasing date.
2. Warranty will be void if the following conditions are found.
   (a) Some modification has been made to this product.
   (b) The product is operated incorrectly (not follow the instruction in this manual).
   (c) The warranty sticker is torn or damaged.

1.6. Support

The support by email about IP Lock problem can be sent to iplock@design-gateway.com. Otherwise, the request on our website is available by following link.

http://www.design-gateway.com/contact.html

Your personal information is restricted with high confidentiality.

2. IP Lock core

2.1. The core operation

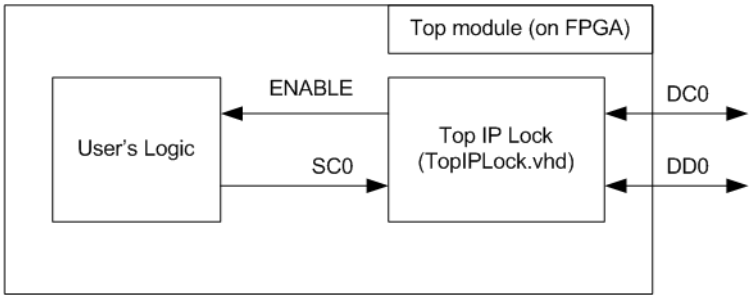


Figure 2-1 IP Lock System

As shown in Figure 2-1, the IP Lock core has four signals for connecting to other modules, i.e. SC0, DC0, DD0, and ENABLE. SC0 is the system clock for running IP Lock core. *The frequency range of SC0 is 1 – 25 MHz*. The DC0 and DD0 are the external I/Os for connecting with IP Lock device. Both signals are bi-directional signals. ENABLE signal is the output of IP Lock core for the user's logic. When the link communication between IP Lock core and IP Lock device is successfully created, ENABLE signal will be asserted to '1'. Otherwise, ENABLE signal is de-asserted to '0' (the communication is failed).

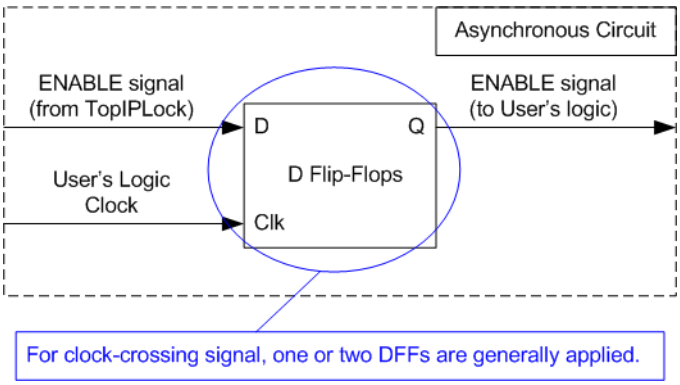


Figure 2-2 Recommended logic for using ENABLE signal

The user's logic can use ENABLE signal to enable the internal operation by monitoring ENABLE to be equal to '1'. It's recommended for the user's logic to add one or two DFFs before using ENABLE signal to be the synchronous circuit, as shown in Figure 2-2.

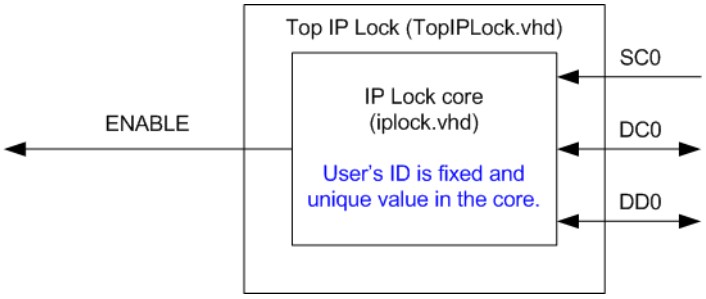


Figure 2-3 Top level of IP Lock

TopIPLock (TopIPLock.vhd) is designed to be the wrapper file of IP Lock core (iplock.vhd) to show the input/output signals of the core. The user's ID in IP Lock core and IP Lock device is fixed and unique in each product box. ENABLE signal is de-asserted to '0' if the user's ID in the IP Lock core is not same as the user's ID in the IP Lock device.

2.2. The license file

To implement the IP Lock core by using FPGA tool (ISE/Vivado for Xilinx device or Quartus for Intel device), the user must send email to iplock@design-gateway.com for generating the IP Lock license file. The information in Figure 2-4 must be sent to email for generating the license file. The user can select to lock the license file by using Volume ID or Network ID.

Name / Company: .....
IP Lock Serial Number: .....
Volume / Network ID: .....
Address: .....
Tel: .....
Fax: .....

Figure 2-4 Information for register

Figure 2-5 shows the command to check Volume ID and Network ID by using Windows command prompt. “getmac” is the command to check Network ID while “dir” is applied to check Volume ID.

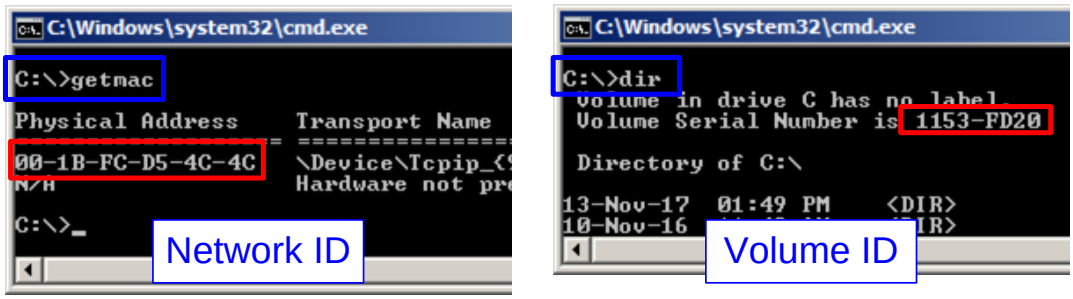


Figure 2-5 Volume Serial Number

After the user gets the license file from Design Gateway, the user must add the license file to the tool license by using text editor. Assume that, “License.lic” is the license file of Xilinx tool (ISE or Vivado) while “License.dat” is the license file of Intel tool (Quartus). Figure 2-6 shows the example to add IP Lock license to Xilinx and Intel tool.

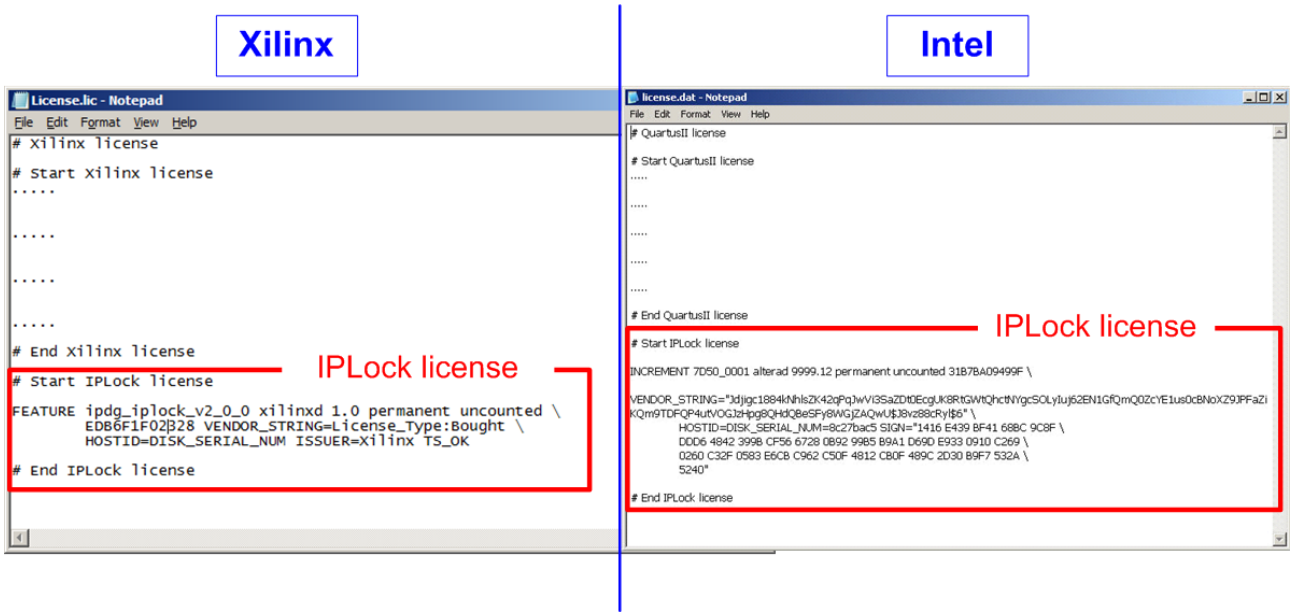


Figure 2-6 Add IP Lock license to the tool's license

2.3. The example VHDL design

The example VHDL code to use IP Lock core is included in the delivery item. The hardware block diagram in the example design is shown in Figure 2-7.

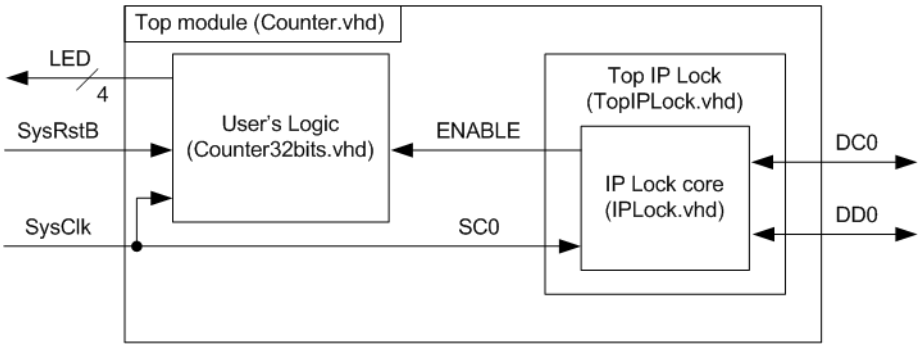


Figure 2-7 Example VHDL design block diagram

Counter.vhd is the top module which includes the example of user's logic and the IP lock core. The example of user's logic is Counter32bits.vhd. The user's logic uses ENABLE signal to be counter enable to blink LED[0] and LED[1] signal. SysClk is applied to be clock input for user's logic and IP Lock core.

The example project to use IP Lock core (IPLock.vhd) in each FPGA tool is shown in Figure 2-8. The IP Lock core is added to the project as the source like other HDL modules.

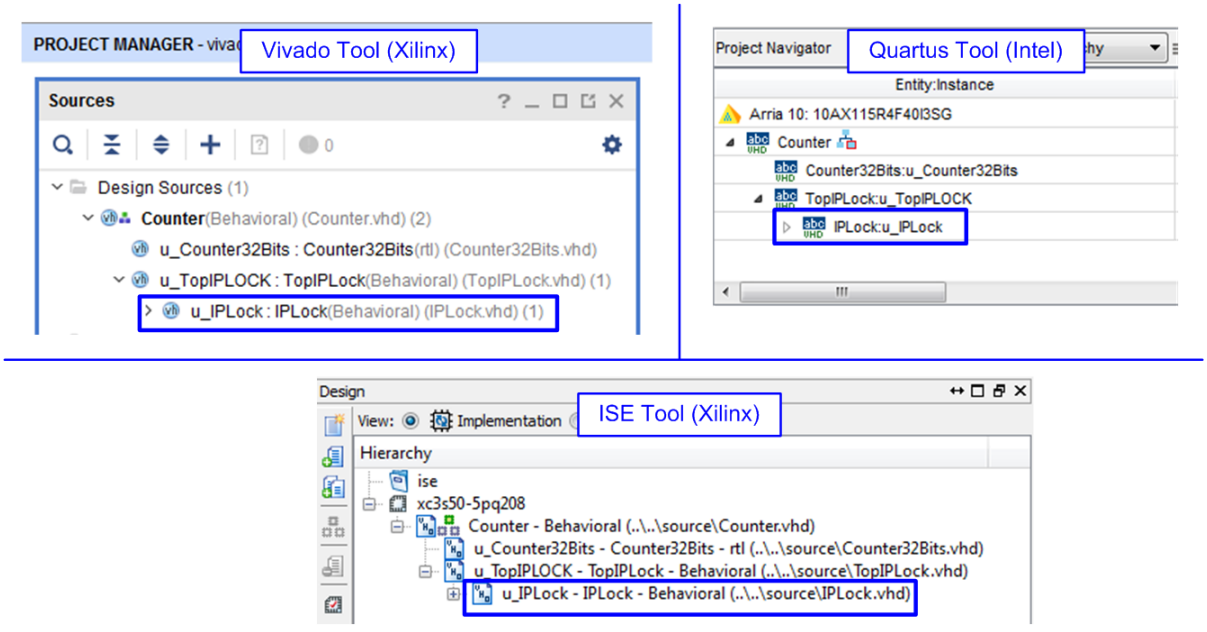


Figure 2-8 Example project for IP Lock core in each FPGA tool

3. IP Lock Device

IP Lock device is designed to communicate with the IP Lock core (implemented within FPGA) to protect FPGA core. The connection between IP Lock device and IP Lock core must be online status. If the communication link is lost, the IP Lock core will change the status of ENABLE signal to '0' to disable the user's logic inside the FPGA.

The hardware connections to use the IP lock device are shown in Figure 3-1 and Figure 3-2. Voltage of IP Lock device and FPGA I/O Voltage for connecting to IP Lock device must be fed from the same source. The supported voltages are +1.8V, +2.5V, and +3.3V.

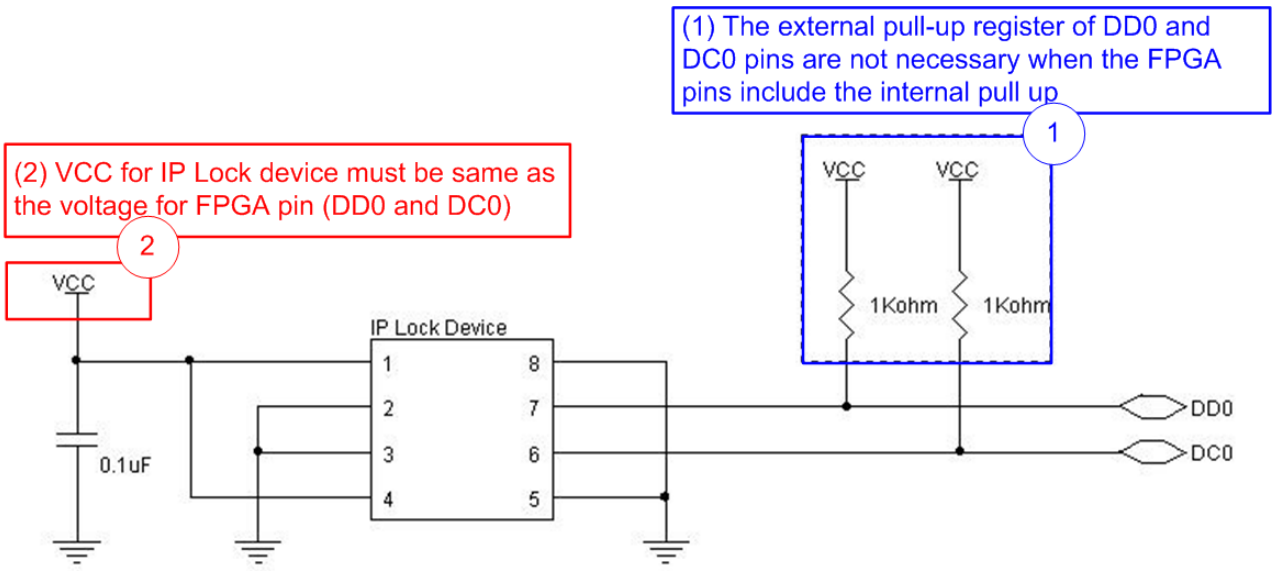


Figure 3-1 IP Lock device connection when internal pull up is not included in FPGA pin

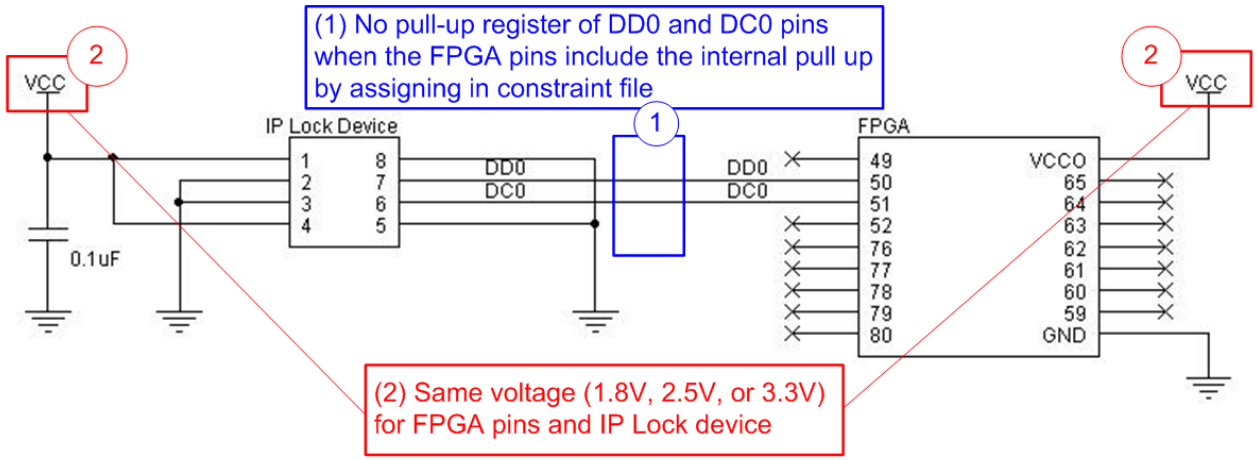


Figure 3-2 IP Lock device connection when internal pull up is included in FPGA pin

The example constraint file to add pull up register for FPGA pin is shown in Figure 3-3. Three examples are shown for three FPGA tools, i.e. ucf file for ISE tool (Xilinx), xdc file for Vivado tool (Xilinx), and qsf file for Quartus tool (Intel).

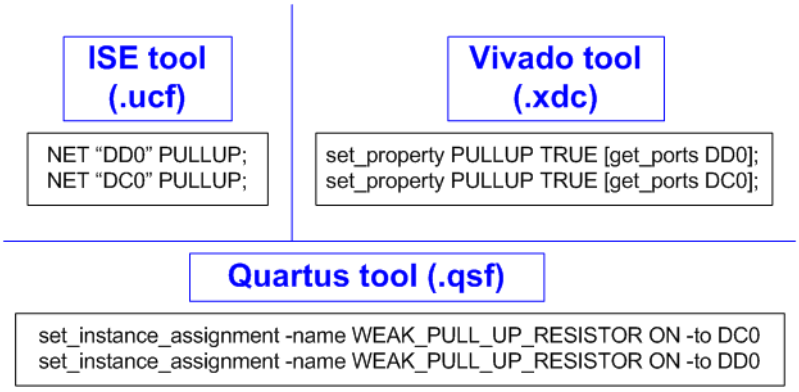


Figure 3-3 Add pull up register to FPGA pin

Note: When the IP Lock core is implemented by Vivado tool, the user must set the additional constraint file to ignore timing constraint for the internal signal of IP Lock core, as shown in Figure 3-4. "u_IPLock" in the example is the component name of IP Lock core, set in TopIPLock.vhd. If the user modifies the component name of IP Lock core within TopIPLock.vhd, the ignore path must be modified to match the new component name.

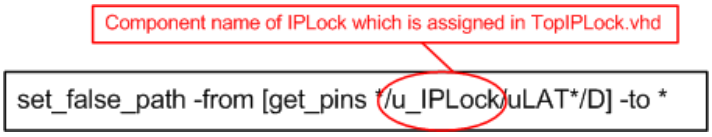
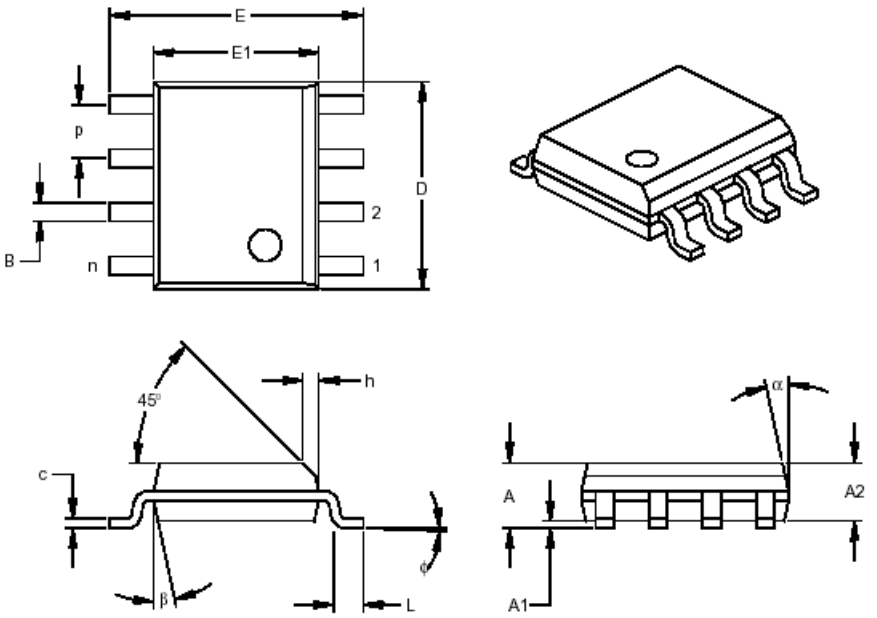


Figure 3-4 Ignore path for Vivado tool

The IP Lock device packages and dimensions are shown in Figure 3-5 and Figure 3-6.



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Figure 3-5 Package dimension of IP Lock device

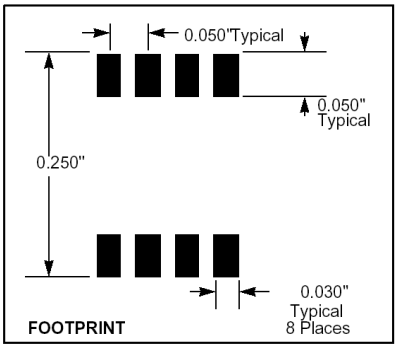


Figure 3-6 Footprint of IP Lock device (all dimensions are in inch unit)

4. Troubleshooting

The following information is the conclusion of some problems which may be found when using the IP Lock product.

Q: Why the ENABLE signal output from IP Lock core is de-asserted to '0'?

A: (1) Please check IP Lock device direction on PCB is mounted correctly.

(2) Please check pin assignment of the FPGA is correct position.

Q: What is the specification of power supply voltage for IP Lock device?

A: Please supply voltage of IP Lock device by using the same source with FPGA I/O pins which are connected to IP Lock device.

Q: Do DD0 and DC0 of IP Lock device need pull up?

A: The user can add the pull up registers on PCB or use the internal pull up by FPGA assignment.

Q: Why the IP Lock core and the IP Lock device must use from the same product box?

A: Because the IP Lock core and the IP Lock device in the standard pack have the user's ID which is the unique value for each product box. If the user's ID it not matched, ENABLE signal will be de-asserted to '0'.

If the above suggestion cannot solve your problem, please contact our support team by using email or sending the inquiry on our website.

IP Lock product support email: iplock@design-gateway.com