

How to transfer design with IPLock from ISE to Vivado

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Introduction

This document describes how to transfer HDL design with IPLock from ISE software to Vivado software. The document contains 3 processes. First process show process to request and change iplock.ngc file to encrypted iplock.vhd. Second process show process for add encrypted iplock.vhd to Vivado software. Third process show process for add IPLock license file to Vivado software.

The encrypted iplock.vhd is more suitable for use with Vivado software than iplock.ngc. However, the implementation encrypted iplock.vhd on Vivado software need IPLock license file.

In this document show example counter project. The sourcecode contains in CD in IPLock package. Counter.vhd is top level and contains 2 components, Counter32Bits.vhd and TopIPLock.vhd. TopIPLock.vhd contains IPLock.vhd (encrypted file).

Process for request encrypted iplock.vhd file and IPLock license file

- 1. Send all this information to email: iplock@design-gateway.com
 - Customer name or contact person name
 - Company name and company address
 - IPLock serial no. (see on IPLock package)
 - MAC address of the computer to be used for the implementation
 - FPGA device part no. or FPGA device family
- 2. Design Gateway check all information.
- 3. Design Gateway send encrypted iplock.vhd and IPLock license file to customer



Process for add encrypted iplock.vhd on Vivado software

This following step is example project to use encrypted iplock.vhd. This project is counter pattern with enable count by iplock. All sourcecode provide in CD.

1. Create project folder that contains 4 subfolders: ip, source, vivado and xdc folder.



Figure 1 Project Folder

- ip folder contains iplock.vhd (encrypt file)
- source folder contains Counter.vhd, Counter32Bits.vhd and TopIPLock.vhd
- vivado folder is project folder
- xdc contain counter.xdc

counter.xdc file is constraints file. The pin constraints and timing constraints need to set in the project as show in Figure 2.



Figure 2 set pin and timing constraints



pin constraints
set_property PACKAGE_PIN H4 [get_ports SysClk]
set_property IOSTANDARD LVCMOS25 [get_ports SysClk]

set_property PACKAGE_PIN K4 [get_ports SysRstB]
set_property IOSTANDARD LVCMOS25 [get_ports SysRstB]

I/O # set_property PACKAGE_PIN H2 [get_ports {LED[0]}] set_property IOSTANDARD LVCMOS25 [get_ports {LED[0]}]

set_property PACKAGE_PIN H1 [get_ports {LED[1]}]
set_property IOSTANDARD LVCMOS25 [get_ports {LED[1]}]

set_property PACKAGE_PIN J2 [get_ports {LED[2]}]
set_property IOSTANDARD LVCMOS25 [get_ports {LED[2]}]

set_property PACKAGE_PIN J1 [get_ports {LED[3]}]
set_property IOSTANDARD LVCMOS25 [get_ports {LED[3]}]

set_property LOC H13 [get_ports DD0] set_property IOSTANDARD LVCMOS25 [get_ports DD0]

set_property LOC H12 [get_ports DC0] set_property IOSTANDARD LVCMOS25 [get_ports DC0]

timing constraints
create_clock -name SysClk -period 200.0 [get_ports SysClk]
set_false_path -from [get_pins */u_IPLock/uLAT*/u_Latch/D] -to *

In constraint file need to set up output pin and pin constraints. Both set up depend on part and board that customer select.



- 2. Open Vivado software then Create Project
- 3. Set project name and project location then click next

New Project					8
Project Name Enter a name for y	our project and specify a direct	ory where the p	roject data files will	be stored.	A
<u>P</u> roject name:	counter				0
Project location:	D:/IPLock/counter/vivado				⊗
Create proje	ct subdirectory				
Project will be cr	reated at: D:/IPLock/counter/viv	ado			

Figure 3 set Project name and Project location

- 4. Select RTL project then click next
- 5. Add source file to project: Counter.vhd, Counter32Bits.vhd, TopIPLock.vhd and IPLock.vhd.

e on disk an	netlist, Block I d add it to you	Design, and IP files, or d Ir project. You can also a	irectories contai idd and create s	ning those files, to add to y ources later.	our	project. Create a new source	
+, -	1 1 4						
	Index	Name	Library	HDL Source For		Location	
•	1	Counter.vhd	xil_defaultlib	Synthesis & Simulation		D:/IPLock/counter/source	
•	2	Counter32Bits.vhd	xil_defaultlib	Synthesis & Simulation	٣	D:/IPLock/counter/source	
•	3	TopIPLock.vhd	xil_defaultlib	Synthesis & Simulation		D:/IPLock/counter/source	
•	4	IPLock.vhd	xil_defaultlib	Synthesis & Simulation	*	D:/IPLock/counter/ip	
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Figure 4 add source file to project



6. Add constraints file to project, counter.xdc. then click next

🔑 New Project	:						
Add Cons Specify or cr	traints eate con	(optional) Istraint files for physical a	nd timing constrain	ts.			4
Constrai counter:	nt File	Location D:IIPLock/counter/vdc					
			Add Files	<u>Create File</u>]		
Copy c	onstrair	its files into project					
হ				< <u>B</u> ack	<u>N</u> ext >	Einish	Cancel

Figure 5 add constraints file to project

7. Select parts or boards then click next

Reset Al	l Filters									
Category	All			Package:	All	✓ Ten	nperature:	All		~
Family:	All			Speed:	All	 ✓ Stat 	ic power:	All		×
Part	S X0730	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra R.	AMs	DSPs	G
xc7s6ft	b196-1	196	100	3750	7500	5	0	7 un 5	10	0
xc7s6ftg	b196-1IL	196	100	3750	7500	5	0		10	0
xc7s6ftg	b196-1Q	196	100	3750	7500	5	0		10	0

Figure 6 select parts or boards



9. Figure 7 show Vivado project after add source file and constraint file

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File Edit Flow Tools Report	s window Lag	aut Aism	Heb -													T Default are	Ready	
		B W														= Default Layor	01	
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		u_IPLock : IPL	ock(Behavioral	(IPLock.vhd)	(63)		Project	location:	D://PLock/c	ounter/vivad	0							
IP INTEGRATOR	~ Constraints	(1)	Counter 328ic	s(m) (counter	32Bills (md)		Produc	t family:	Spartan-7	-								
Create Block Design	~ 😑 constra	1 (1)					Top m	part. odule name:	Counter	10-1								
Open Block Design	Cour	nter.xdc					Target	language:	Verilog									
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	▷ impl_1	constrs_1	Not started											Vivado Implementation Defaults (Vivado	o Implementation 2019)	Vivado Implementation Default Report	nts (Vivado Im	

Figure 7 Vivado software

10. Figure 8 show source file structure



Figure 8 source file structure



- 11. Click Generate Bitstream and wait.
- 12. Figure 9 show Vivado synthesis and implementation complete



Figure 9 Vivado synthesis and implementation complete



Process for add IPLock license file to Vivado software

The Vivado software need IPLock license file to implementation encrypted iplock.vhd. The customer can receive IPLock license file by send customer information and MAC address to email: <u>iplock@design-gateway.com</u>. After receiving IPLock license file, customer can add them to Vivado software by following this step.

- 1. Open Vivado software.
- 2. Tool bar, click Help then select Manage License...
- 3. At Vivado License Manager Window, select Load License as shown in Figure 10

Vivado License Manager 2019.2	
VIVADC	License Manager
Get License Get Set Proxy Gotol License Manage License Manage License Munage License Search Paths Wew Viscense Status View Wost License Information Wiew Host Information	Load License Certificate Based Licenses Circlificate Based Licenses Circlificate Based Licenses Circlificate based licenses (.i.c file) into the %APPDATA%\VilimxLicense directory. Xilinx applications automatically detect valid, node-locked licenses (*.i.c) residing in the %APPDATA%\VilimxLicense directory. Copy License

Figure 10 Load IPLock license file

4. Select IPLock license file

🦢 Vivado License Manager 2019.2		
File Help		
VIVADO.	License Manager	€ XILINX
GetLicense	Load License	
Ce	tificate Based Licenses	î
Load License Manage License Manage License Manage License	e File	ense directory. Xilinx hse directory.
View License Status	: 🚺 CoreLicenses 🔹 🗸 🧊 📰 🗸	
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Figure 11 Select IPLock license file



Figure 12 show IPLock license file was installed successful.

Vivado License Manage	er 2019.2	
	License Manager	€ XILINX
Get License God License Manage License Manage License Wew Vicense Status View West Information View Host Information	Load License Certificate Based Licenses Click the 'Copy License' button to copy a certificate-based license (.ic file) into the %APPDATA% VilinxLicense dire applications automatically detect valid, node-locked licenses (*.ilc) residing in the %APPDATA% VilinxLicense dire Copy License	rectory. Xilinx ctory.
	Vivado License Manager Vivado License installation was successful: C:\Users\Pook\AppData\Roaming\XilinxLicense\ipdg_iplock_v1_0_0_flexIm.lic OK	

Figure 12 Load IPLock license file successful

5. IPLock license file was shown in Vivado License Manager

See Vivado License Manager 2019.2 File Help		Manager	7			ı – ı XIL	■ ¤
Get License Get Proxy Gotan License License Michael License Michael License	Certificate Based Licen	ses:	View	License Status	Filter:	V Hide Free Built-in Li	censes
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Figure 13 Vivado License Manager show IPLock license file

6. complete