How to transfer design with IPLock from ISE to Vivado

Design Gateway Co., Ltd. 5 Apr 2022

Introduction

This document describes how to transfer HDL design with IPLock from ISE software to Vivado software. The document contains 3 processes. First process show process to request and change iplock.ngc file to encrypted iplock.vhd. Second process show process for add encrypted iplock.vhd to Vivado software. Third process show process for add IPLock license file to Vivado software.

The encrypted iplock.vhd is more suitable for use with Vivado software than iplock.ngc. However, the implementation encrypted iplock.vhd on Vivado software need IPLock license file.

In this document show example counter project. The sourcecode contains in CD in IPLock package. Counter.vhd is top level and contains 2 components, Counter32Bits.vhd and TopIPLock.vhd. TopIPLock.vhd contains IPLock.vhd (encrypted file).

Process for request encrypted iplock.vhd file and IPLock license file

1. Send all this information to email: iplock@design-gateway.com
   - Customer name or contact person name
   - Company name and company address
   - IPLock serial no. (see on IPLock package)
   - MAC address of the computer to be used for the implementation
   - FPGA device part no. or FPGA device family
2. Design Gateway check all information.
3. Design Gateway send encrypted iplock.vhd and IPLock license file to customer

Process for add encrypted iplock.vhd on Vivado software

This following step is example project to use encrypted iplock.vhd. This project is counter pattern with enable count by iplock. All sourcecode provide in CD.

1. Create project folder that contains 4 subfolders: ip, source, vivado and xdc folder.

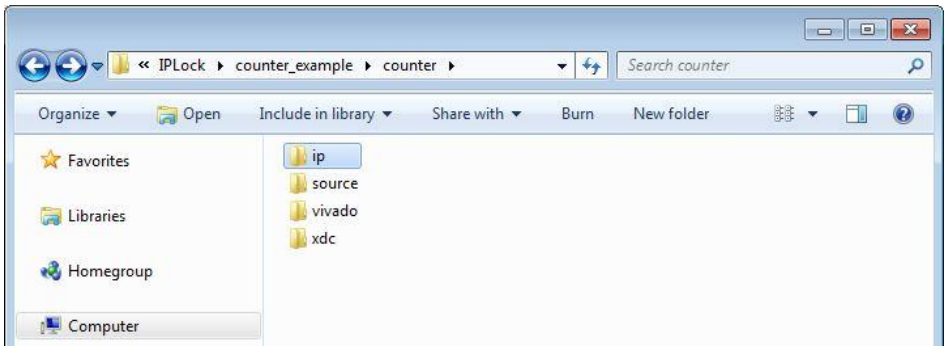

Figure 1 Project Folder

- ip folder contains iplock.vhd (encrypt file)
- source folder contains Counter.vhd, Counter32Bits.vhd and TopIPLock.vhd
- vivado folder is project folder
- xdc contain counter.xdc

counter.xdc file is constraints file. The pin constraints and timing constraints need to set in the project as show in Figure 2.

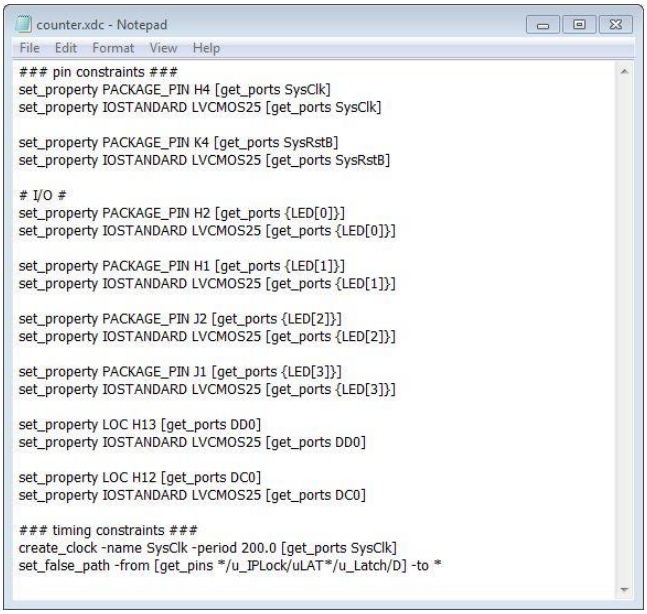

Figure 2 set pin and timing constraints

```
### pin constraints ###
set_property PACKAGE_PIN H4 [get_ports SysClk]
set_property IOSTANDARD LVCMOS25 [get_ports SysClk]

set_property PACKAGE_PIN K4 [get_ports SysRstB]
set_property IOSTANDARD LVCMOS25 [get_ports SysRstB]

# I/O #
set_property PACKAGE_PIN H2 [get_ports {LED[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports {LED[0]}]

set_property PACKAGE_PIN H1 [get_ports {LED[1]}]
set_property IOSTANDARD LVCMOS25 [get_ports {LED[1]}]

set_property PACKAGE_PIN J2 [get_ports {LED[2]}]
set_property IOSTANDARD LVCMOS25 [get_ports {LED[2]}]

set_property PACKAGE_PIN J1 [get_ports {LED[3]}]
set_property IOSTANDARD LVCMOS25 [get_ports {LED[3]}]

set_property LOC H13 [get_ports DD0]
set_property IOSTANDARD LVCMOS25 [get_ports DD0]

set_property LOC H12 [get_ports DC0]
set_property IOSTANDARD LVCMOS25 [get_ports DC0]

### timing constraints ###
create_clock -name SysClk -period 200.0 [get_ports SysClk]
set_false_path -from [get_pins */u_IPLock/uLAT*/u_Latch/D] -to *
```

In constraint file need to set up output pin and pin constraints. Both set up depend on part and board that customer select.

2. Open Vivado software then Create Project
3. Set project name and project location then click next

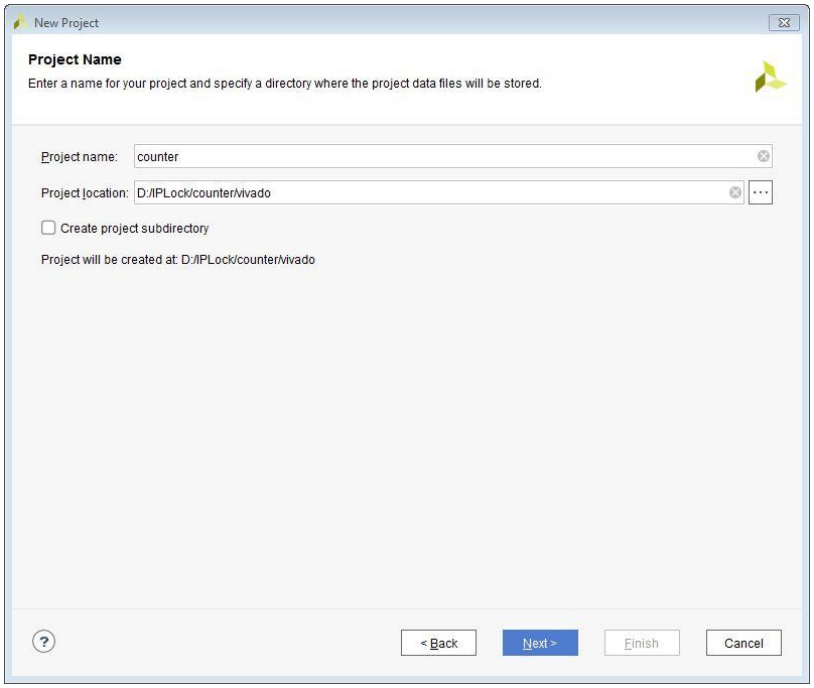

Figure 3 set Project name and Project location

4. Select RTL project then click next
5. Add source file to project: Counter.vhd, Counter32Bits.vhd, TopIPLock.vhd and IPLock.vhd.

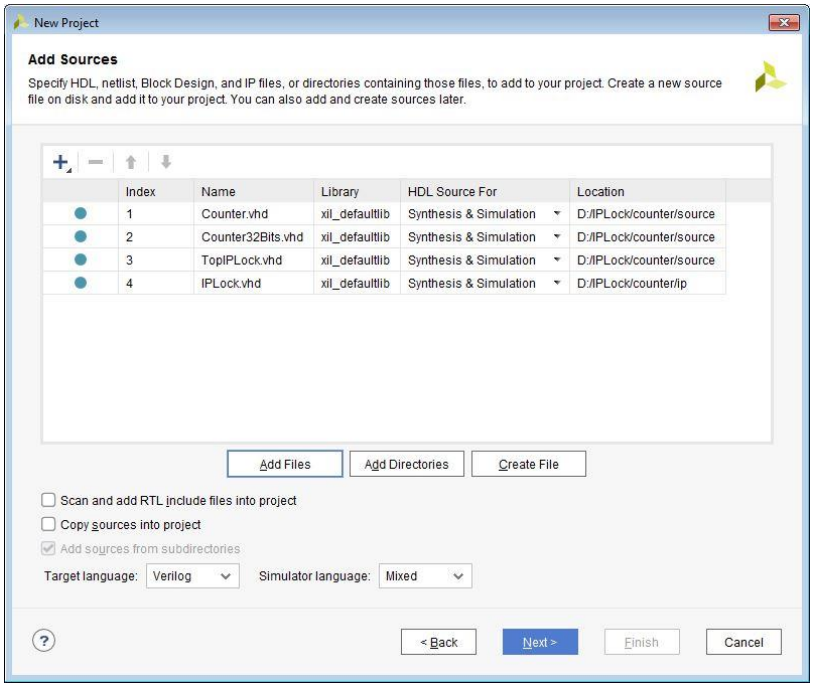

Figure 4 add source file to project

6. Add constraints file to project, counter.xdc. then click next

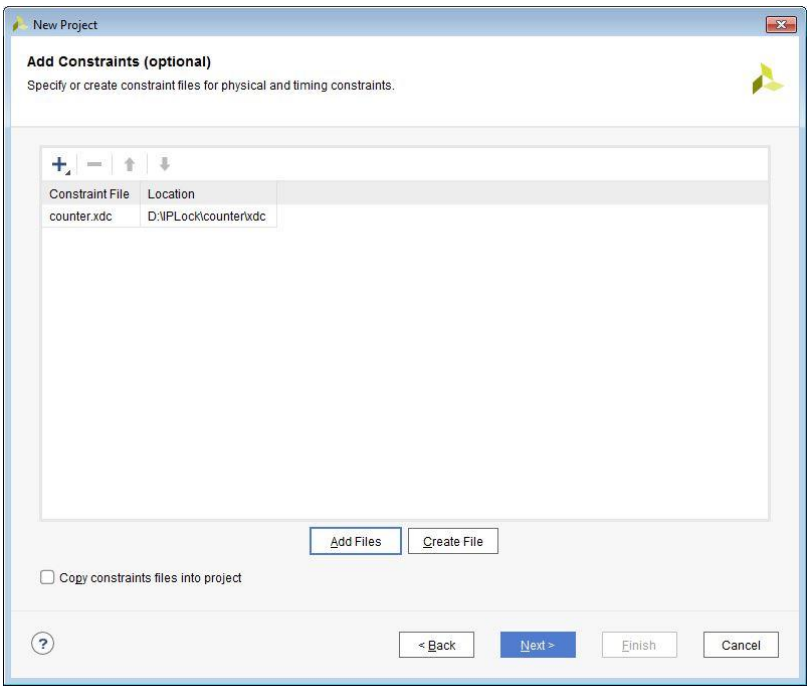

Figure 5 add constraints file to project

7. Select parts or boards then click next

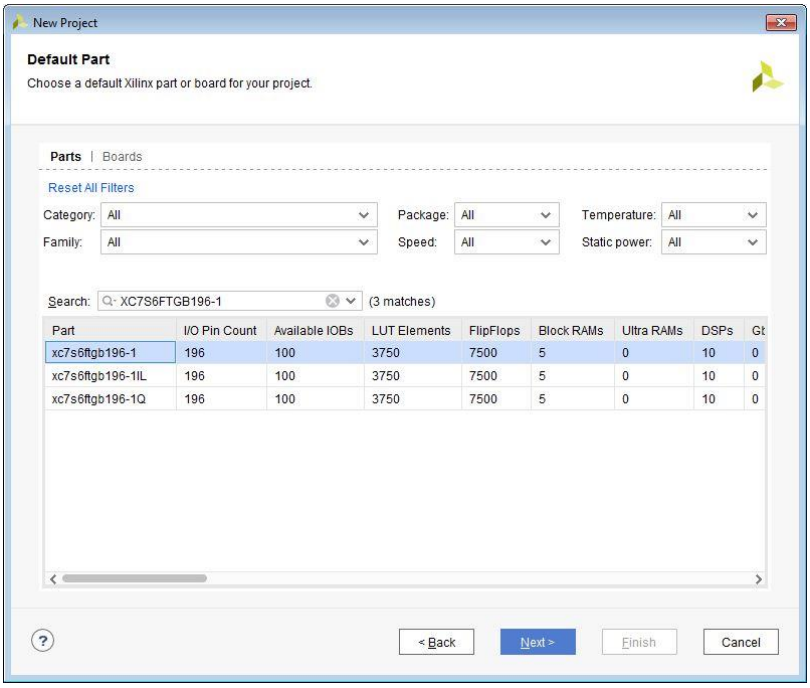

Figure 6 select parts or boards

8. Click Finish to create project

9. Figure 7 show Vivado project after add source file and constraint file

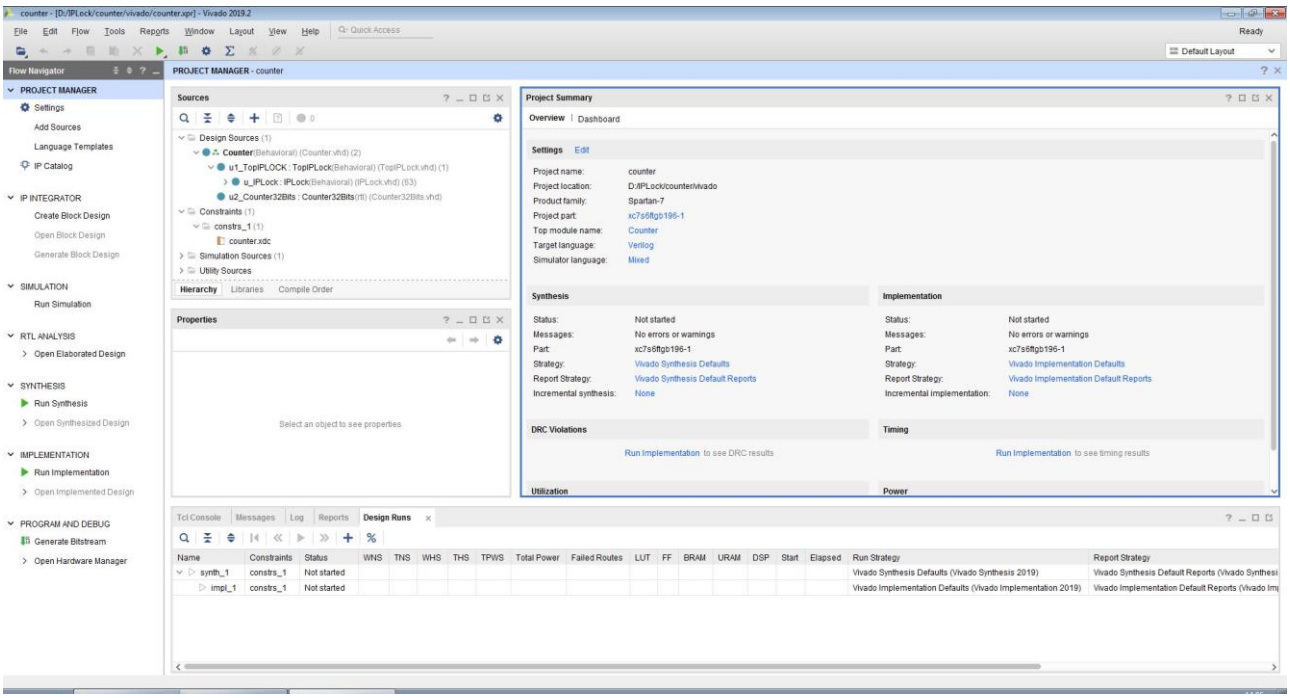

Figure 7 Vivado software

10. Figure 8 show source file structure

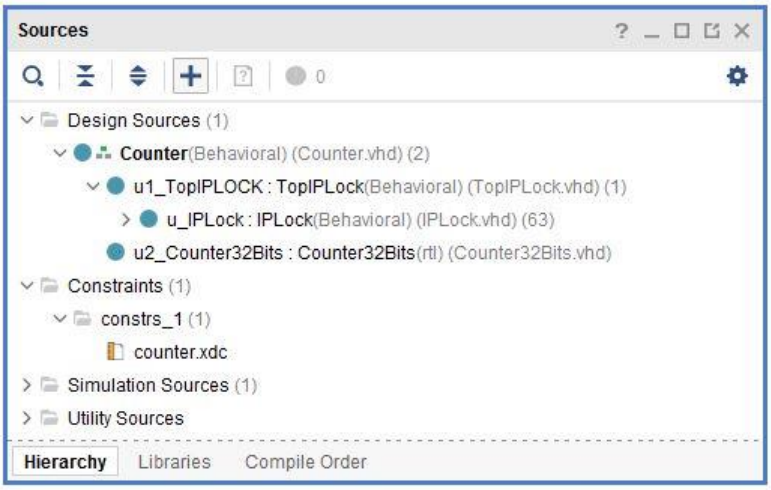

Figure 8 source file structure

11. Click Generate Bitstream and wait.

12. Figure 9 show Vivado synthesis and implementation complete

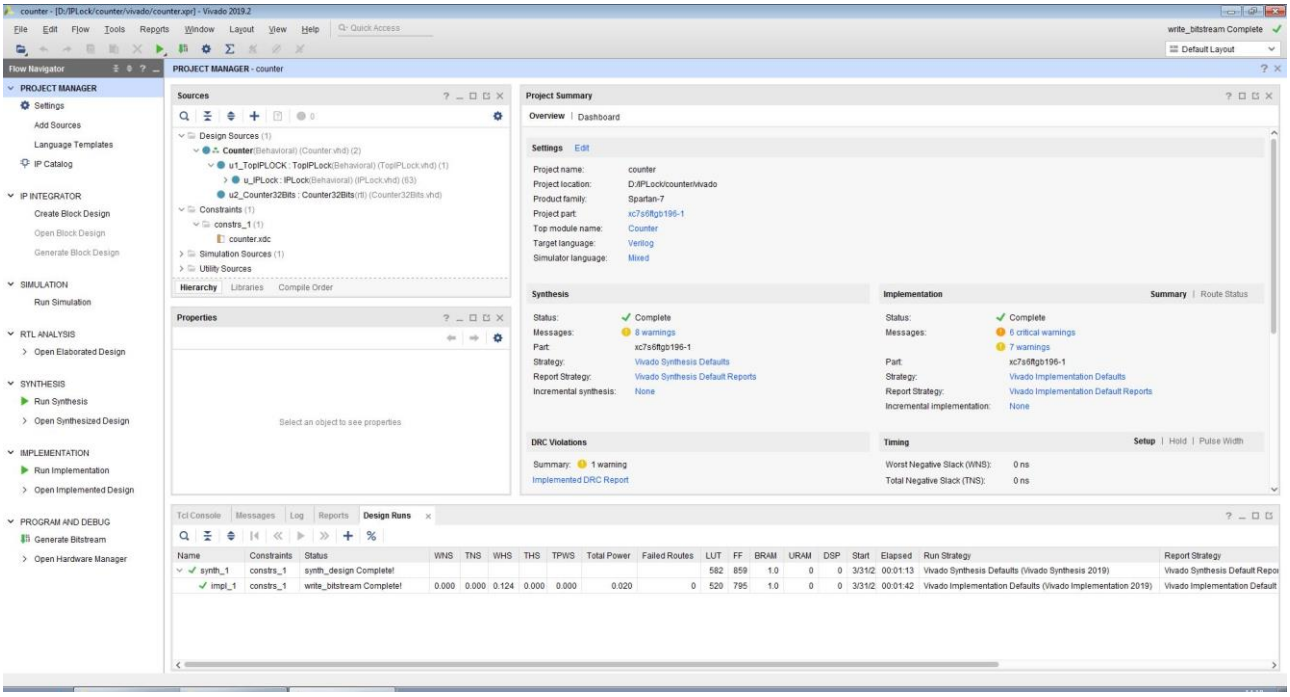

Figure 9 Vivado synthesis and implementation complete

Process for add IPLock license file to Vivado software

The Vivado software need IPLock license file to implementation encrypted iplock.vhd. The customer can receive IPLock license file by send customer information and MAC address to email: iplock@design-gateway.com. After receiving IPLock license file, customer can add them to Vivado software by following this step.

1. Open Vivado software.
2. Tool bar, click Help then select Manage License…
3. At Vivado License Manager Window, select Load License as shown in Figure 10

Figure 10 Load IPLock license file

4. Select IPLock license file

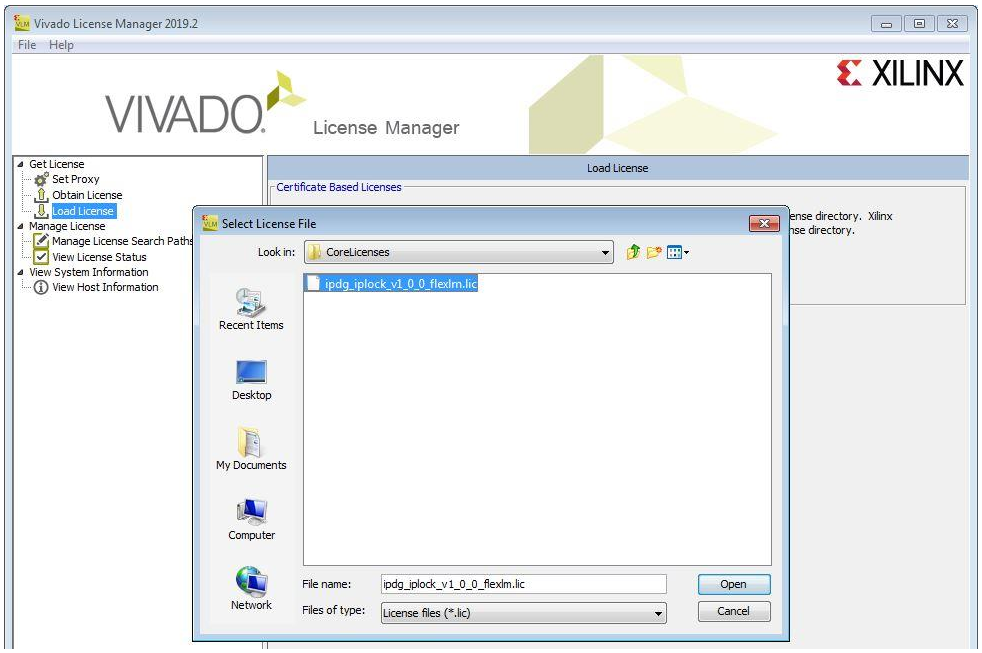

Figure 11 Select IPLock license file

Figure 12 show IPLock license file was installed successful.

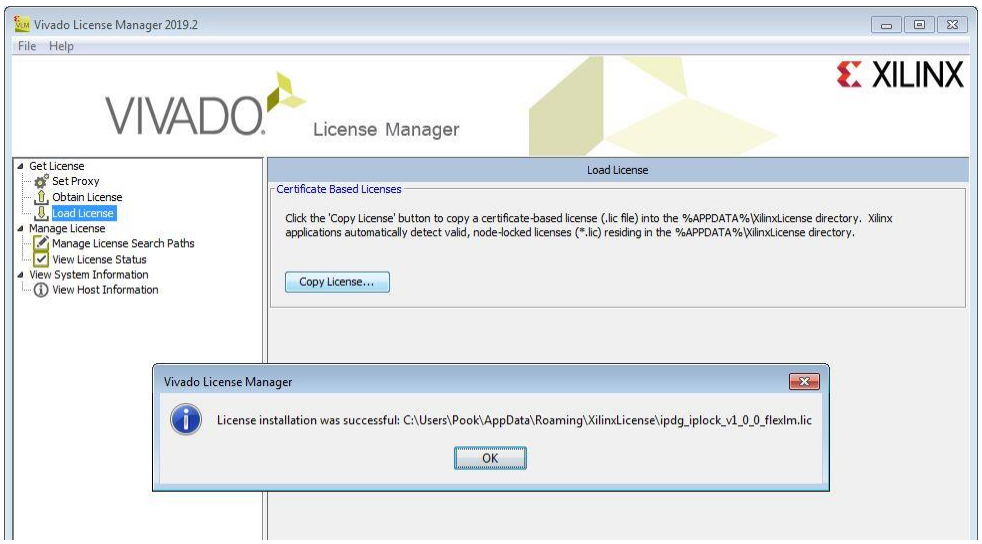

Figure 12 Load IPLock license file successful

5. IPLock license file was shown in Vivado License Manager

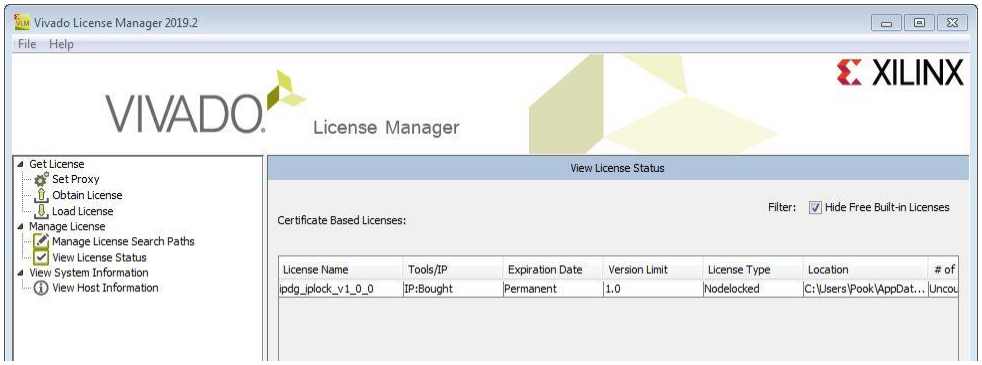

Figure 13 Vivado License Manager show IPLock license file

6. complete