EMBEDDED SOLUTIONS CATALOG

AMD Adaptive SoCs / FPGAs Zero-CPU Solutions

Eliminate CPU/OS Bottlenecks with Design Gateway's
Full Hardware Acceleration Technology

- AMD Versal™ Powered Real-Time Data Capture & FTP Transfer
- Sustained 7,000 MB/s NVMe Storage Acceleration on Embedded Linux for Zynq® UltraScale+™ MPSoC
- Ultra-High-Speed Network & Security Offloading for AMD Kria™ SOM
- Accelerated Algorithmic Trading on Alveo™ X3522PV Nano-Level HFT Solution

DESIGN GATEWAY COMPANY LIMITED

Design Gateway Co., Ltd.

The Expert of IP Core & Zero-CPU Hardware Acceleration Solutions

AMD Embedded Partner Network GOLD

AMD Versal™ Powered Real-Time Data Capture & FTP Transfer

Eliminate CPU overhead and expensive, proprietary hardware with Design Gateway's **full hardware-accelerated data processing suite**. Engineered for AMD Versal™, this unified solution offloads the complete 100G TCP/IP and FTP stacks into programmable logic—delivering deterministic real-time capture, NVMe storage, and remote streaming. Running seamlessly over standard, long-distance network fabrics, it provides a scalable, **zero-CPU** pipeline adaptable to mission-critical applications such as radar systems, high-performance test & measurement, medical imaging, and HPC cluster processing.

UPLOAD 5,400 MB/s

DOWNLOAD 4,100 MB/s

Why CPU-Based System Fall Short

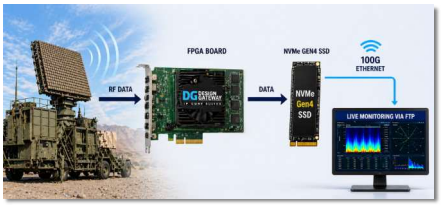
- Continuous Data Recording Bottleneck
- TCP/IP Processing Bottleneck
- exFAT File System Performance Constraint
- System Downtime for NVMe Data Retrieval

Why Choose Versal Powered Zero-CPU Solution

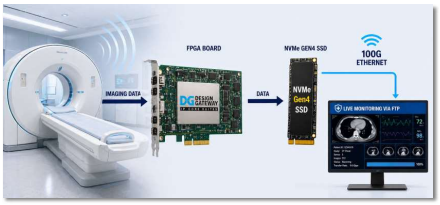
- Deterministic Continuous Recording
- Hardware-Offloaded Real-Time TCP/IP Processing
- Scalable exFAT File System Acceleration
- Non-Disruptive Remote Data Access

Ideal for Mission-Critical Applications

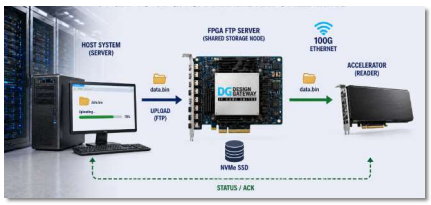
Designed for mission-critical applications that demand high-speed performance, stable operation, real-time processing, and reliable file access.



RF Data Logging with Real-time Monitoring



CT Scan & High-Resolution Imaging



Host-System Connection for HPC

FPGA Data Logging System with Live FTP Monitoring

FPGA-Based FTP Server Delivers 5,400+ MB/s Speed

Sustained 7,000 MB/s NVMe Storage Acceleration on Linux for Zynq UltraScale+ MPSoC

In conventional FPGA-based embedded Linux systems, the processing overhead of generic NVMe drivers and PCIe Gen3 limitations often restricts modern NVMe SSD performance to around 1,600 MB/s.

By combining Design Gateway's **fully hardware-based NVMe-IP** with a PCIe Gen4 SSD, FPGA SoC platforms can achieve **over 7,000 MB/s** of sustained raw-data write performance.

- **Sequential Access**
- **Zero CPU Usage**
- **Zero-Copy Memory**
- **Up to 7,000 MB/s**

Ideal for Applications Requiring High Performance Data Recording with Zero CPU Usage

Aerospace & Defense

Medical Instruments

Media & Entertainment

Test and Measurement

Breaking the Embedded Linux Barrier: 6,300 MB/s Random File Access

Traditional OS file systems severely degrade NVMe performance during non-sequential storage tasks. Our Zero-CPU storage architecture overcomes this, delivering an unprecedented **6,300 MB/s sustained file write speed** even under demanding **random file access** workloads—all with near-zero CPU utilization.

Ideal for Applications Requiring High Computational Load and Massive Data Throughput

AI Interface Systems

Autonomous Systems

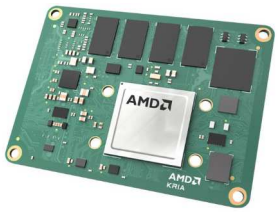
Edge Computing

Video Analysis & Image Processing

Breakthrough NVMe Performance on Zynq UltraScale+:
7 GB/s with NVMe Gen4 IP on PetaLinux

From 1,600 MB/s to 6,300 MB/s:
Four Keys to High-Performance NVMe File Access
on FPGA-based Linux

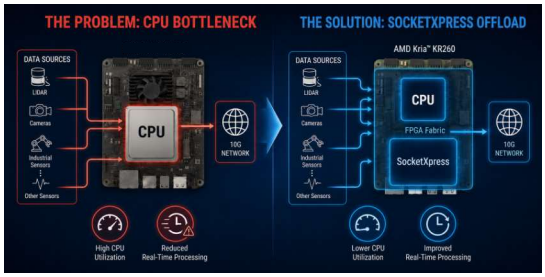
Ultra-High-Speed Network & Security Offloading for AMD Kria™ SOM



Stop Software Bottlenecks in Edge Applications

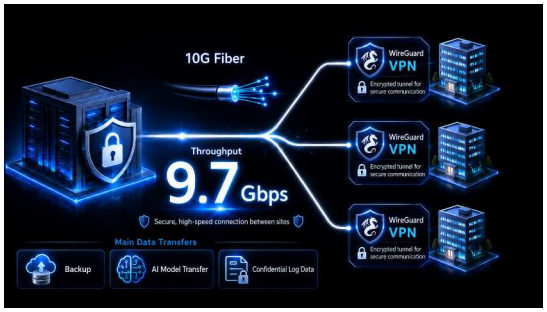
On platforms like the AMD Kria KR260, the Linux TCP/IP stack caps at ~3 Gbps under load, consuming precious CPU cycles needed for AI or control workloads. **SocketXpress** intercepts standard POSIX socket calls and redirects them to a dedicated FPGA TCP Offload Engine—unlocking up to **9.4 Gbps** with **zero code changes**.

Zero CPU | **Zero Code Changes** | **9.4 Gbps TCP speed**



HW Accelerated WireGuard for Full 10G Secure Links

Standard software VPNs throttle 10GbE enterprise links due to the massive CPU load of real-time encryption. **WireGuard10G-IP** solves this by executing the entire protocol directly in hardware logic, achieving full 10 Gbps line-rate throughput with **zero CPU load** and no external memory. This deterministic, secure Full 10G Link is the ideal infrastructure for high-bandwidth corporate environments requiring daily data backups between headquarters and branch offices, seamless local AI model transfers, and real-time secure data logging.



Zero-CPU QUIC Solutions for Unstable Wireless Links

Eliminate OS Bottlenecks and Packet Loss in 5G/6G, Satellite, and Edge Networks with Full Hardware Acceleration. Software-based TCP and QUIC both suffer catastrophic performance drops. **Pure hardware QUIC-IP** shatters this limitation — maintaining 80% transfer efficiency even under a harsh 10% packet loss rate, and sustaining 8 Gbps throughput under severe out-of-order packet conditions.

80% efficiency at 10% packet loss | **8 Gbps under Out-of Order**

Autonomous Drone Control over 5G/6G Networks

QUIC-IP enables fast, reliable real-time communication for precise autonomous control, even over unstable 5G/6G networks.

Accelerated Algorithmic Trading on Alveo™ X3522PV and UL3524 Nano-Level HFT Solution

FinoLogic

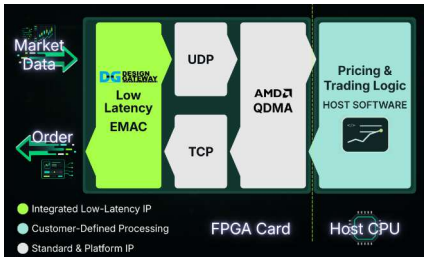
Accelerate High-Frequency Trading with the FinoLogic AAT Solution on FPGA, built on a market-proven ultra-low-latency IP foundation. The system receives real-time market data via UDP, processes it through a configurable pricing engine (deployable on-card or in host software), and executes orders via TCP, all while maintaining sub-microsecond latency.

FinoLogic AAT Solution on FPGA supports multiple development flows and flexible pricing-engine deployment to reduce latency and shorten time-to-market. Select the flow that best fits your team—ITCH/OUCH, QDMA, Calypte, or Vitis —and scale seamlessly from prototype to production.

Gateway

Starter FPGA Architecture

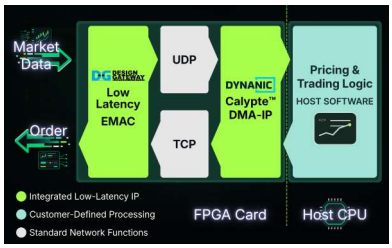
RTT 7us



Leverages **LL10GEMAC-IP** to deliver a highly cost-effective entry point for low-latency Ethernet acceleration, all while preserving your existing host-based trading software.

Configurable FPGA-Based AAT Architecture Options

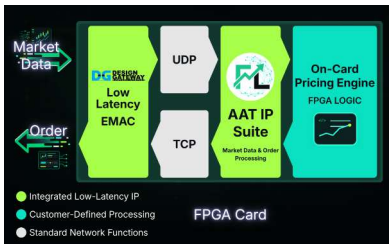
Flexible HFT Architectures Tailored to Your Algorithmic Strategies



FLEXIBLE

Hybrid Architecture

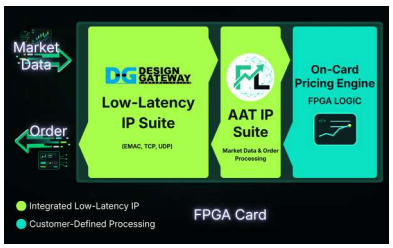
Offloads Ethernet and DMA to FPGA while keeping pricing and trading logic on the host.



RECOMMENDED

On-Card Architecture

Executes AAT and pricing entirely on-card to eliminate critical-path host round trips.



FULLY OPTIMIZED

Complete Low-Latency Architecture

Maximizes latency reduction by integrating the full AAT and DG Low-Latency IP suites on-card.

RTT 5us ▸ Cuts Latency 87% ▸ RTT 650ns ▸ Cuts Latency 43% ▸ RTT 370ns

Key Components

Core Building Blocks of the Low-Latency HFT

LL 10GEMAC-IP
for Core Networking

Tx 18.6ns
Cuts Latency 10.2ns
Rx 21.7ns
Cuts Latency 3.9ns

* Vs. AMD Ethernet MAC

UDP10GLL-IP
for Datagram Transport

Tx 6.2ns
Rx 37.2ns
Cuts Latency 29.5ns

* Vs. HLS UDP

TOE10GLL-IP
for Session Transport

Tx 6.2ns
Cuts Latency 257ns
Rx 46.5ns

* Vs. HLS TCP

AMD Alveo UL3524
Ultra-Low Latency Card

GTF 17.06ns
Cuts Latency 48ns

* UL3524 (16-bit @ 644 MHz) vs. X3522 with DG LL10GEMAC-IP + GTY (32-bit @ 322 MHz).

Enabling High-Performance IP Product Line

As an industry-leading expert in Hardware Logic design and IP Cores, Design Gateway provides highly reliable, field-proven components. Coupling these with AMD Adaptive SoCs and FPGAs offers an accelerated track to deploying robust Zero-CPU environments.

Key IP Core Portfolio

Categoly	IP Core	Core Properties
Storage	・NVMe-IP ・SATA-IP ・NVMeTCP-IP	Enables CPU-free direct drive access and multi-drive RAID. Unleashes highest possible Versal and Zynq UltraScale+ bandwidths.
Networking	・TOE-IP ・UDP-IP ・QUIC-IP ・WireGuard-IP ・Low Latency Networking IPs	Full wire-speed hardware packet handling from 1G to 200G.
Security	・TLS1.3-IP ・tCAM-IP ・AES256-GCM-IP ・AES256-XTS IP ・ECDSA256 IP ・SHA3-IP ・ChaCha20-Poly1305 IP	Executes line-rate data encryption and decryption, offering robust security fully optimized for DG storage and network IP cores.

Why Design Gateway?

As an established AMD Embedded Partner, we deliver fully validated reference designs alongside deep engineering support. We provide support for the latest devices, offering tailored special and advanced reference designs optimized for real-world applications.

DESIGN GATEWAY COMPANY LIMITED

Head Office

3-23-17 Naka-cho, Koganei, Tokyo, JAPAN

https://dgway.com

R&D

89/26 Amornpan 205 Tower1, 18th floor, Ratchadapisek 7, Ratchadapisek Road, Din Daeng, Bangkok, 10400 THAILAND

https://design-gateway.com